Application Design with the Bitsy Compact Flash Interface

ADS document # 110111-80022

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Revision History

ADS document # 110111-80022:

REV	DESCRIPTION	DATE	BY
1	Initial Document Generation		
2	Updates - Corrected number of CF address bits to 11		

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1 Introduction

The Bitsy Single Board Computer contains a Compact Flash electrical interface. The signals which comprise this interface are routed to an expansion connector on the board. The intent is that this interface could be routed to a standard Compact Flash connector on a separate daughter board or utilized as a general purpose expansion port for the CPU. This expansion port can then be used to interface various peripherals required for a particular application that could not be included on the original Bitsy platform such as Ethernet, expanded discrete I/O, serial ports, etc. The focus of this paper is this type of design application. This paper will present a description of the Compact Flash interface, a reference design, and an interface timing analysis. It is expected that the reader has some experience with digital logic design and a basic understanding of the StrongArm microprocessor.

2 Compact Flash Overview

The Compact Flash specification consists of an electrical and mechanical standard. Electrically, the Compact Flash Interface is defined by an 11 bit address bus, a 16 bit data bus, various control signals, and several miscellaneous signals which have specific definitions for use with Compact Flash cards. The interface is asynchronous with access timing defined by a software in a programmable register. For slower devices the cycle can be extended by asserting a handshake signal. The specification divides the host address space into three regions: I/O, Attribute, and Memory. The I/O space supports addressing to 8 or 16 bit devices. The Memory and Attribute space assumes that only 16 bit devices are connected. Two sets of read and write control signals are provided which are asserted based on what region is being addressed. Several signals are provided in the specification which can be utilized as interrupt inputs. A voltage level signal is provided to allow support for 3.3 or 5V signal levels.

3 Host Interface

The Bitsy Single Board Computer contains a StrongArm SA1110 Microprocessor and SA1111 Companion Chip. The SA1111 provides support for the Compact Flash interface. The SA1111 decodes the microprocessor access to the Compact Flash region of memory and asserts the appropriate signals on the Compact Flash interface. This provides very good signal integrity through the connector to the daughter card.

4 Application Design Example

Figure 1 illustrates an example circuit with supports a 16 bit Ethernet device and an 8 bit serial port with variable waitstate timing. Programmable logic is included to support chip decoding and signal polarity translation.

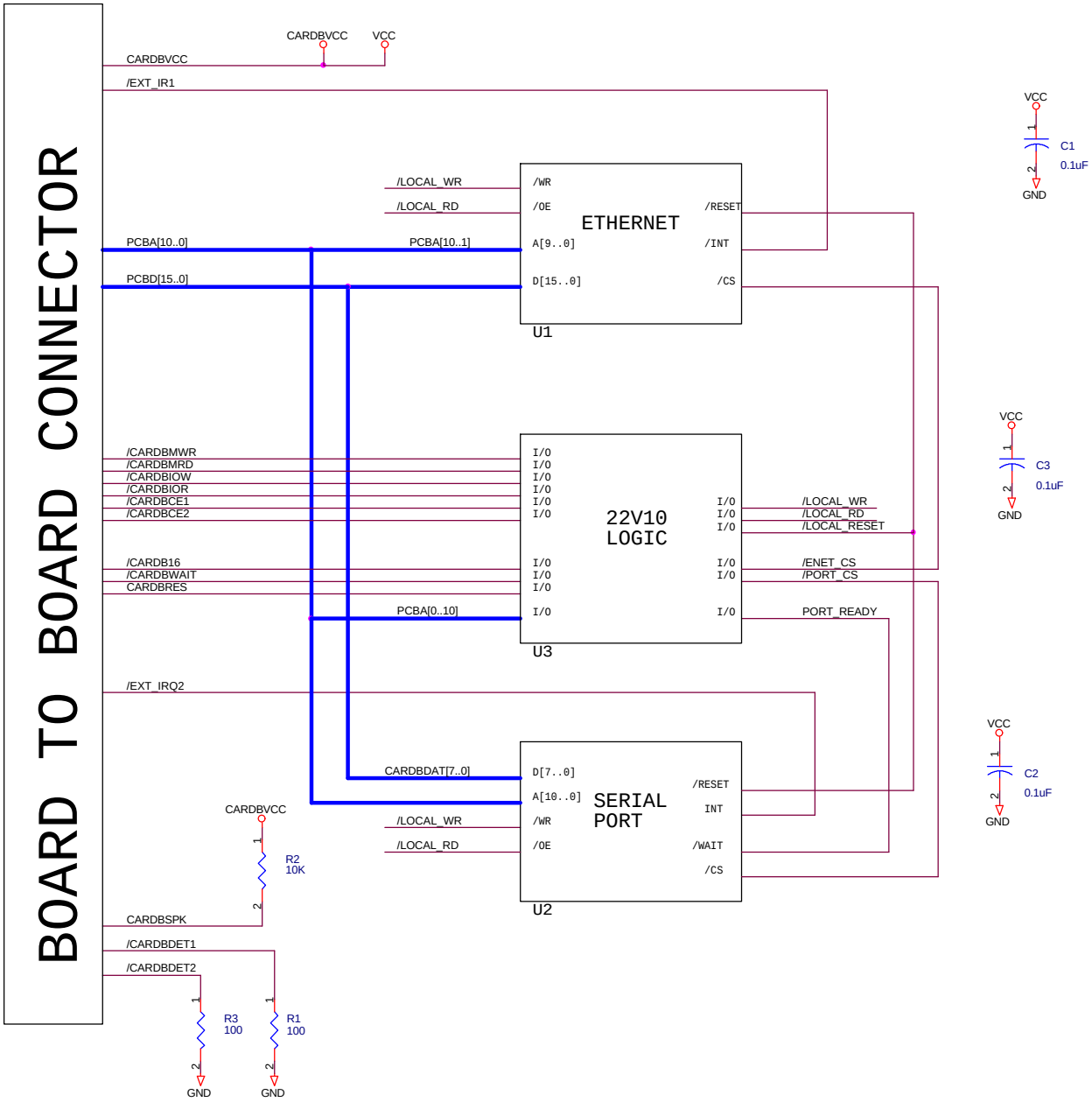

Figure 1 – Reference Design Circuit

The design example includes support for 8 and 16 bit device connection, address decoding, and variable latency control. In this example, 5V devices were selected, so CARDBVCC is connected to the VCC (5V) plane. If 3.3V devices were used, this signal would subsequently be connected to the 3.3V plane. The signal pull-ups must be tied to the voltage level of the Compact Flash Interface. Note that CARDBSPK must be terminated through a pull-up if this interface is used. If mixed voltage devices were required, some isolation buffers would be required to protect the lower voltage devices from the high voltage logic.

Since unique read and write lines are used, the chip select inputs of both chips can be tied to the enabling logic state. Another option is to tie them to /CARDBCE1. Signals /CARDBDET1 and /CARDBDET2 must be tied to Ground to enable the interface on the Bitsy Board. Signal /CARDB16 is pulled high because the Serial Port is an 8 bit device. If this were a 16 bit device, then /CARDB16 would have to be Grounded. Additional devices could be connected in this manner and would require only a small amount of glue logic to provide address decoding to generate chip selects. Additional connections are provided from the Bitsy Single Board Computer which are not shown in the design example. These lines can be used to support interrupts or provide discrete signaling between the Bitsy and the daughtercard. Variable latency is supported by driving the /CARDBWAIT signal low then high to complete the cycle. If the device used doesn't provide a signal of this polarity, then additional logic will be required to invert the signal.

5 Timing

The interface timing can be completely under host software control using the SA1110 MECR register. The MECR register is divided to provide unique software timing control for accesses to I/O, Memory, and Attribute space. For most applications this will be sufficient. If variable timing is required as is shown in the design example, connect the device ready signal to /CARDBWAIT. While /CARDBWAIT is driven low, additional waitstate cycles will be inserted in addition to those programmed in the MECR register.

In this example suppose that the Ethernet device has an access time of 30ns and the serial port requires variable waitstates with the Ready signal active low within 100ns of the start of the cycle. The SA1110 MECR register bits 31..16 would be loaded with 0x8002 to generate a 48ns cycle for access to the Ethernet device, and 125ns cycle for access to the Serial Port. An access to the Serial Port would not terminate until the device deasserted its /WAIT pin. The designer should refer to the detailed timing requirements of the devices actually used and program the MECR register according to the deign guidelines in the Intel SA1110 Developer's Manual.

6 Bitsy Connector Pinout

Bitsy board connectors J15, 16, and 17 collectively provide all of the signals that would be required to support the design example circuit. Please refer to the Applied Data Systems Bitsy User's Manual for more information about pinout and connector type.

7 Support Documentation

The following documentation will provide more detailed information about the StrongArm microprocessor, the Compact Flash interface, and the Bitsy Single Board Computer.

Intel StrongArm SA-1110 Mircoprocessor Advanced Developer's Manual, order number: 278240-003

Intel StrongArm SA-1111 Microprocessor Companion Chip Developer's Manual, Order Number: 278242-003

Applied Data Systems Bitsy User's Manual, Document Number 110111-1003x