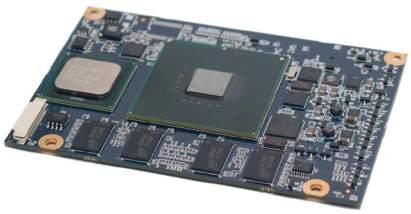
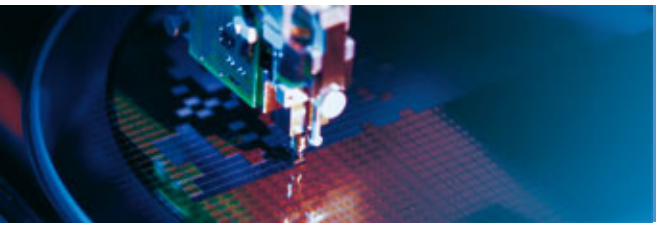
DESIGN–IN GUIDE





Catalyst Module and Catalyst Module XL

Rev. 3 March 2010

DIGITAL TECHNOLOGIES FOR A BETTER WORLD

www.eurotech.com

EUROTECH

Disclaimer

The information in this document is subject to change without notice and should not be construed as a commitment by any Eurotech company. While reasonable precautions have been taken, Eurotech assumes no responsibility for any error that may appear in this document.

Trademarks

All product or service names are the property of their respective owners.

Revision History

Issue no.	*PWB*	*Date*	*Comments*
1		Nov-2008	Initial release
2		Dec-2009	Catalyst Module XL information added Power Requirements section updated SDVO recommendations updated TPM supported as optional feature
3		March-2010	Board Revision section updated Backlight signal descriptions clarified Low power state table updated

For contact details, see page 55.

Contents

Introduction 4
Handling Your Board Safely 5
Conventions 5
Features 7
Catalyst Module and Catalyst Module XL 7
Software Specification 9
Operating System Support 9
Drivers 9
BIOS 9
Hardware Specification 10
Block Diagram 10
Core Processor 10
Memory 12
Communications 14
User Interface and Display 17
Inputs and Outputs 19
Intel High Definition Audio 20
Power Requirements 20
Carrier Board Design 27
Test and Debug 30
Mechanical 30
Connectors, LEDs, and Jumpers 34
Identifying Connectors 34
Signal Headers 35
J1: Docking Connector: Data 35
J2: Docking Connector: Power 42
J3: ITP Debug Port 43
System Specifications 44
Performance 44
Power 44
Electrical 46
General 48
Environmental 48
Appendix A – Reference Information 49
Appendix B – RoHS Compliance 50
Appendix C – Board Revision 51
Appendix D – Development Kit 53

Introduction

The Catalyst Module is a high-performance, low-power module based on the Intel® Atom™ processor. It uses an integrated two-chip solution comprised of the Intel Atom processor and Intel® System Controller Hub US15W (Intel® SCH US15W). The Intel Atom processor utilizes the new low-power Intel micro architecture, while the Intel SCH US15W contains an integrated 2D/3D graphics controller supporting hardware-accelerated graphics display and video processing capabilities. The Catalyst Module allows embedded users to gain higher performance with greater energy efficiency.

An application-specific carrier board integrates with the Catalyst Module for a total production solution. This flexible, modular architecture enables easy customization and quick time-to-market. A Eurotech carrier board is available that implements several industry-standard interfaces allowing development across a broad spectrum of end-use applications. This design provides a reference for unique carrier boards optimized for high-performance, low-power applications such as ruggedized handheld, multimedia, medical, point of service, and industrial designs.

The Catalyst Module supports the following interfaces:

- LVDS display
- Serial Digital Video display
- Backlight with control signals for intensity and on/off
- Integrated system BIOS with external BIOS support
- IDE/PATA interface
- Two PCIe x 1 busses
- Eight USB 2.0 ports
- Three SD/MMC interfaces
- SMBus
- I^2C bus with I^2C master device
- LPC bus
- Two general-purpose inputs and outputs
- Intel® High Definition Audio

This guide provides details about the various features of the Catalyst Module and about how they create a system that meets your application needs. It extends the information provided in the Catalyst Module Development Kit User Manual and is intended for hardware design engineers. Design details are provided as guidelines for custom carrier board design.

Unless specified otherwise, the information in this guide applies to the Catalyst Module and Catalyst Module XL. For board revision history, see Appendix C – Board Revision, page 51.

Handling Your Board Safely

Anti-Static Handling

The Catalyst Module contains CMOS devices that could be damaged by electrostatic discharge (ESD). Observe industry-standard electronic handling procedures when handling the module. Where possible, work on a grounded anti-static mat. At a minimum, touch an electrically grounded object before handling the module or touching any components on the module.

Packaging

Please ensure that, should a module need to be returned to Eurotech, it is adequately packed, preferably in the original packing material.

Electromagnetic Compatibility

The Catalyst Module is classified as a component with regard to the European Community Electromagnetic Compatibility (EMC) regulations. Because Eurotech supplies only the single-board computer and not fully integrated systems, Eurotech cannot provide meaningful system-level emissions test results. It is the responsibility of the user to ensure that systems using the module are compliant with the appropriate EMC standards.

RoHS Compliance

The European RoHS Directive (Restriction on the use of certain Hazardous Substances – Directive 2002/95/EC) limits the amount of six specific substances within the composition of the product. The Catalyst Module fully complies with the RoHS directive. A full *RoHS Compliance Materials Declaration Form* for the Catalyst Module is included as Appendix B – RoHS Compliance, page 50. Further information regarding RoHS compliance is available on the Eurotech web site at www.eurotech.com.

Conventions

The following table lists the symbols that are used in this guide.

Symbol	Explanation
	Note – information that requires your attention
	Warning – proceeding with a course of action may damage your equipment or result in loss of data

The following table describes the conventions that specify the mode of a register.

Symbol	Explanation
RW	Readable and writable register
RO	Read only register

The following table describes the conventions that specify signal names.

Convention	Explanation
GND	Digital ground plane
#	Active low signal
+	Positive signal in differential pair
-	Negative signal in differential pair

The following table describes the abbreviations that specify direction and electrical characteristics of a signal.

Type	Explanation
I	Signal is an input to the system
O	Signal is an output from the system
IO	Signal may be input or output
P	Power and ground
A	Analog signal
OD	Open-drain
CMOS	3.3 V CMOS
LVCMOS	1.05 V CMOS
LVTTL	Low Voltage TTL
3.3	3.3 V signal level
5	5 V signal level
IDE	5 V tolerant signal
HDA	3.3 V (default) or 1.5 V signal
HCSL	Host Clock Signal Level
LVDS	Low Voltage Differential Signaling
PCIe	PCI Express signal
PWM	Pulse Width Modulation
nc	No connection
reserved	Use is reserved to Eurotech

Some signals include termination on the Catalyst Module. The following table describes the abbreviations that specify the signal termination.

Termination	Explanation
PU	Pull-up resistor to the specified voltage
PD	Pull-down resistor
R	Series resistor
C	Series capacitor

Features

Catalyst Module and Catalyst Module XL

Processor

- Intel® Atom™ processor
- Intel System Controller Hub US15W
- Clock rates from 1100 MHz to 1600 MHz
- Front side bus from 400 MHz to 533 MHz

Integrated System Functions

- Trusted Platform Management (optional)
- Embedded Controller

Memory

- 512 MB, 1 GB, or 2 GB DDR-2 DRAM
- Integrated system BIOS with external BIOS support
- Battery-backed real-time clock
- External memory support
  - IDE/PATA disk drive
  - USB disk drive
  - SD/MMC card
  - PCI Express card

Communications

- Two PCI Express one lane interfaces
- Eight Universal Serial Bus 2.0 ports
  - Up to six host ports operating at low, full, and high speeds
  - Two host ports operating at high speed only
  - One client port operating at high speed
- Three Secure Digital and MultiMediaCard interfaces
- System Management Bus interface
- I^2C bus with I^2C master device

User Interface and Display

- Two independent display outputs
  - LVDS with resolutions up to 1366 x 768 at 85 Hz, 8-bit color per lane
  - Serial Digital Video with resolutions up to 1280 x 1024 at 85 Hz, full color
- Backlight interface with control signals for intensity and power

Inputs and Outputs

- Low Pin Count bus for general-purpose I/O expansion
- Two general-purpose inputs and outputs

Audio Interface

- Intel High Definition Audio supporting up to two external audio codecs

Power Supply

- 3.3 V and 5 V main power inputs
- Low power consumption
- ACPI power management

Mechanical

- 67mm x 100mm dimensions
- Less than 10mm total stack height

Environmental

- Extended operating temperature
- No external cooling required
- RoHS compliant

Software Specification

Operating System Support

The Catalyst Module is compatible with the following operating systems:

- Windows® XP Professional
- Windows XP Embedded
- Windows Embedded Standard
- Windows CE 6.0
- Linux
- Select real-time operating systems

Drivers

System components have drivers available for the Windows operating system and Linux.

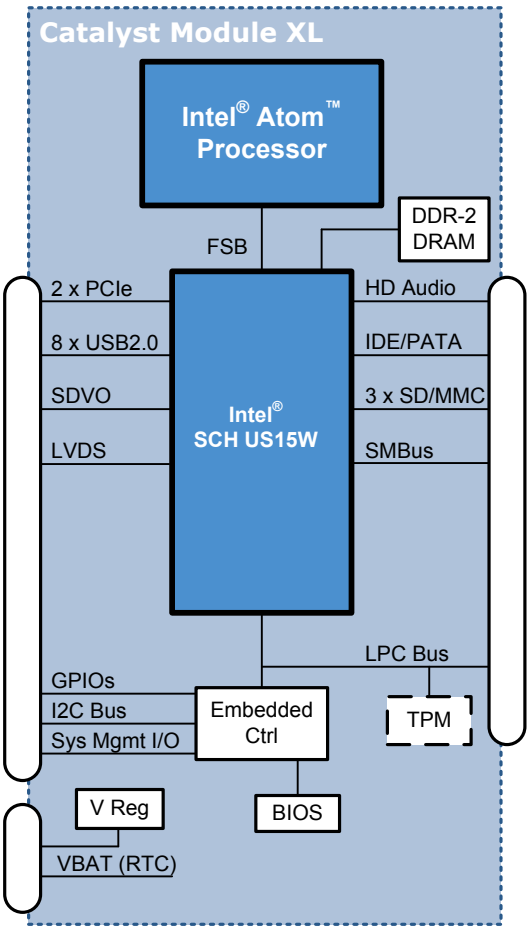
BIOS

The Catalyst Module incorporates a custom system BIOS developed by Eurotech.

Hardware Specification

Block Diagram

The following diagram illustrates the system organization of the Catalyst Module. Notice that the data connector has been divided into two sections for this illustration. The TPM is shown with dotted lines indicating that this is an optional feature supported on the Catalyst Module XL only.



Core Processor

The Catalyst Module bases its architecture on an integrated two-chip solution comprised of the Intel Atom processor and Intel SCH US15W. In addition, the Catalyst Module fully integrates system functions that include Trusted Platform Management (TPM) for industry-standard secure data encryption, system management and control implemented by an advanced chip level solution, tightly integrated power management controls, and system BIOS firmware memory. This fully integrated and flexible feature set increases product readiness and compliance. The following sections describe the functionality and feature set of this processor technology as it relates to the Catalyst Module architecture.

Intel Atom Processor

At the core of the Catalyst Module is the Intel Atom processor that incorporates the new low-power Intel micro architecture. The Intel Atom processor executes the x86 instruction set along with extensions for SSE, SSE2, and SSE3. This processor is built on a 45 nm process using a high-K substrate.

The following are key features of the Intel Atom processor:

- Multi-threading support using Hyper-Threading Technology
- Intel Virtualization Technology
- New “in-order execution” instruction pipeline and simplified decode/branch prediction
- New macro-operations that extend per clock effective instruction execution pipeline width to 2-wide and execute up to four instructions per clock cycle when combined with Hyper-Threading Technology
- Extended dynamic power management using new enhanced Intel SpeedStep® technology “C6” low-power states

See Performance, page 44 for further details about the processor performance.

The Catalyst Module provides several sources for external interrupts. The following table lists each interrupt source with a description of its function. Notice that the GPIO1, GPIO2, and SMB_ALERT# signals have multiple functions. You can access these functions through the BIOS. Refer to the manual for your operating system for details about how the processor handles interrupts.

Interrupt Signal	J1 Pin	Function
IDE_IRQ	A53	IDE/PATA interrupt
GPIO1 GPIO2	A108 A3	System control interrupt or non-maskable system management interrupt
LPC_SERIRQ	A39	LPC bus interrupt
SMB_ALERT#	A33	Non-maskable system management interrupt or additional capability as wake event
PCIE_WAKE#	B55	Standard I/O device wake event signal
PCIE Port 0 PCIE Port 1		PCIe message-based interrupts

Intel System Controller Hub US15W

The Intel Atom processor operates in conjunction with the Intel SCH US15W. This companion device provides a wide range of capabilities that include a 2D/3D graphics controller, PCIe x1 busses, USB ports, SD/MMC interfaces, Intel HD Audio support, an IDE/PATA interface, SMBus, and a RTC function. Subsequent sections describe how the Catalyst Module uses each capability.

Trusted Platform Management (optional)

The optional on-module TPM function is compliant with the Trusted Computer Group specification version 1.2. This function provides public key generation, public key storage encryption/decryption, storage of hashes, key endorsement, and TPM initialization. The Catalyst Module XL supports the TPM on the LPC bus.

Embedded Controller

An embedded controller included on the Catalyst Module performs three main functions: standard firmware hub (FWH) logic emulation, ACPI power management, and hardware monitoring. See Electrical, page 46 for further details about the external I/O signals provided by the embedded controller.

Combined with the system BIOS memory, the embedded controller provides logic emulation of standard FWH functions. It connects to the Intel SCH US15W using the LPC bus and to the system BIOS memory using a serial peripheral interface (SPI). See Non-Volatile Memory, page 12 for a description of the system BIOS memory.

As a second function, the embedded controller supports ACPI power management. It ensures proper start-up, shutdown, and power saving transitions by sequencing the voltages. To manage the input power voltages, the embedded controller provides power state signals to the carrier board and receives a power valid signal from the carrier board. See Power Requirements, page 20 for further details about power management.

Lastly, the embedded controller provides hardware monitoring for temperature and voltage. Temperature monitoring measures temperatures on the Intel Atom processor die and near the memory chips. Voltage monitoring measures the input power and on-module voltage regulators. These functions are accessible using the I^2C bus provided on connector J1. See I^2C Bus, page 16 for further details about the I^2C bus.

Memory

The Catalyst Module combined with a carrier board provides a variety of storage capabilities. The following sections describe the different types of memory supported and provide details about implementation.

Synchronous DRAM

Double Data Rate Synchronous DRAM (DDR-2) is used on the Catalyst Module for system main memory and frame buffer memory. Standard modules include 512 MB with 1 GB and 2 GB options available. The data bus supports 64-bit accesses with a maximum burst bandwidth of 4.2 GB/s (8 B @ 533 MHz). The memory bus operates at the same frequency as the front side bus. See Performance, page 44.

The Intel Atom processor supports unified memory architecture in which the integrated 2D/3D graphics controller memory is “unified” with the system main memory. The default frame buffer is 4 MB with an 8 MB option. BIOS Setup settings select the frame buffer size. Extended graphics memory space is available up to 256 MB. The graphics driver controls this size based on usage.

Non-Volatile Memory

The Catalyst Module includes non-volatile memory for system BIOS storage and a real-time clock (RTC) functionality. The system BIOS options include an on-module system BIOS memory with an external BIOS device supported on a carrier board.

BIOS and Configuration Data

A serial interface flash memory device stores the BIOS boot firmware, BIOS Setup settings, and module configuration data on the Catalyst Module. Standard configuration is 1 MB. The flash device performs logically as a firmware hub (FWH) and connects to the on-module embedded controller using a serial peripheral interface (SPI). This system BIOS memory supports pre-programmability at the device level, in-circuit programming on module, and updates using a run-time flash utility. In addition, programmable write protection is available using multiple flash sectors.

As an alternate FWH implementation, the Catalyst Module supports an external BIOS option on the carrier board. The external device connects to the LPC bus. Two signals, CLK_LPC_FWH (J1 pin A36) and FWH_WP# (J1 PIN A2), are reserved for the optional external BIOS option. The signal CLK_LPC_FWH provides the clock for the external BIOS memory. Connect this signal to one load on the carrier board. See Design Constraints, page 27 for routing guidelines.

The input signal, THERM_ALERT, enables the external BIOS device as the boot memory. This signal controls decode of FWH cycles on the LPC bus and allows an external BIOS device to assume the BOOT address. When THERM_ALERT is driven low immediately preceding de-assertion of the system reset signal, RESET#, the on-module system BIOS memory assumes the FWH ID 1 location and the external BIOS device assumes the FWH ID 0 location. The THERM_ALERT signal has dual purposes and functions as an over-temperature indicator also. See System Management, page 20 for further details.

Real-Time Clock

The Intel SCH US15W includes a RTC function. It retains the system date and time when the system is powered down as long as the 3.3 V “always” power or backup power is provided to the chip. See Power Requirements, page 20 for further details.

External Memory Interfaces

Four types of external memory interfaces provide mass storage options on a carrier board. The Intel SCH US15W supplies an IDE/Parallel ATA (PATA) interface, eight USB ports, three SD/MMC interfaces, and two PCIe x 1 busses that can connect external memory to the Catalyst Module. Connector J1 provides the signals for each option.

The primary source for mass storage is through the IDE/PATA interface that supports up to two devices: one master and one slave. A common application is to connect this interface to a 2.5-inch IDE/PATA disk drive. See Design Constraints, page 27 for routing guidelines.

The following table lists supported IDE/PATA Standards and Modes.

IDE/PATA Standard	Transfer Modes Supported	Transfer Rate (Mbps)
ATA-1 (ATA, IDE)	PIO modes 0, 1, 2 Single-word DMA modes 0, 1, 2 Multi-word DMA mode 0	3.3, 5.2, 8.3 2.1, 4.2, 8.3 4.2
ATA-2, ATA-3 (EIDE, Fast ATA)	PIO modes 3, 4 Multi-word DMA modes 1, 2	11.1, 16.6 13.3, 16.6
ATA/ATAPI-4 (Ultra DMA, Ultra ATA)	Ultra DMA modes 0, 1, 2 (a.k.a. Ultra DMA/33)	16.7, 25.0, 33.3
ATA/ATAPI-5 (Ultra-DMA, Ultra ATA)	Ultra DMA modes 3, 4 (a.k.a. Ultra DMA/66)	44.4, 66.7
ATA/ATAPI-6 (Ultra-DMA, Ultra ATA)	Ultra-DMA mode 5 (a.k.a. Ultra DMA/100)	100 (reads), 89 (writes)

As a second option, an USB disk drive can connect to one of eight USB ports on the Catalyst Module. Any USB device that has USB drivers installed on the Catalyst Module can connect to the USB host ports. See Universal Serial Bus, page 15 for a description of these ports.

Next, you can use a SD/MMC interface to implement a SD/MMC socket on a carrier board providing mass storage. See Secure Digital and MultiMediaCard, page 15 for details about using the SD/MMC interfaces.

Lastly, a PCIe x1 memory card can connect to one of two PCIe x1 busses available on the Catalyst Module. See PCI Express Bus, page 14 for a description of the PCIe capability.

Communications

The Catalyst Module supports several industry-standard channels for communication with peripheral and peer devices. These include PCIe x1, USB, SD/MMC, SMBus, and I^2C bus. The Intel SCH US15W provides the PCIe x1, USB, SD/MMC and SMBus signals, and the embedded controller supplies the I^2C signals. The Catalyst Module does not limit flexibility by integrating fixed function I/O components. All communication signals are available on connector J1 providing flexibility and ease of implementation on the carrier board. This allows development of a unique carrier board optimized for your requirements.

PCI Express Bus

A key capability of the Catalyst Module is its PCI Express one lane (PCIe x1) support. The Intel SCH US15W includes two PCIe x1 interfaces that support 2.5 Gbps bandwidth in each direction. These high-speed differential pairs require strict routing constraints on the carrier board and AC coupling. See Design Constraints, page 27 for routing guidelines.

An on-module clock generator supplies the PCIe clocks for each interface. Additional input signals, PCIEx_CLKREQ#, control each reference clock. On the carrier board, these signals connect to the PCIe slots indicating the presence of a PCIe device. When activated, this signal enables the PCIe clock for the device. See Electrical, page 46 for further details.

Universal Serial Bus

The Intel SCH US15W provides eight Universal Serial Bus (USB) ports. Six ports, USB0-5, function as general-purpose USB host ports and include over-current detection inputs. These ports support the USB 1.1 specification operating at low (1.5 Mbps) and full (12 Mbps) speeds and the USB 2.0 specification operating at high speed (480 Mbps). Use these ports to connect to devices external to the carrier board. USB mouse and keyboard are the most common client devices, but you can connect any USB device that has USB drivers installed on the Catalyst Module.

The two remaining USB ports, USB6 and USB7, operate at high speed only and do not support general-purpose USB host operation. These ports do not support the USB 1.1 specification, and connector J1 does not provide the associated over-current detection signals. When possible, connect these ports to devices on the carrier board.

In order to create a fully functioning USB host port, include the host power supply, current limiter circuits, EMI chokes, and over-voltage protection on the carrier board. See Design Constraints, page 27 for routing guidelines. The USB protocol allows client devices to negotiate the power they need from 100 mA to 500 mA in 100 mA increments. The carrier board must supply the 5 V power required by client devices. Use a power switch with the corresponding over-current detection for each port.

As an optional configuration, USB2 is capable of operating as a USB client port at high speed only. USB client devices are self-powered or can receive power from the host computer. Since the USB cable does not power the Catalyst Module, it does not need a power input. However, the USB input power is useful for sensing when a USB cable is connected. Use the input signal USB_CLIENT (J1 pin B53) to detect a USB cable connection. When a client is connected, this pin should be connected to a 4.7kΩ pull up resistor to 3.3 V on the carrier board. When the port is used as a host port or no client is connected, this signal should be actively driven low on the carrier board.

Secure Digital and MultiMediaCard

The Catalyst Module includes three Secure Digital and MultiMediaCard (SD/MMC) interfaces for memory and I/O expansion. You can use these interfaces to implement a SD/MMC socket on a carrier board providing mass storage or to develop customer unique add-in cards. One interface, SD/MMC2, provides 8-bit operation, while the remaining two interfaces, SD/MMC0 and SD/MMC1, provide 4-bit operation.

These SD/MMC interfaces support the following specifications:

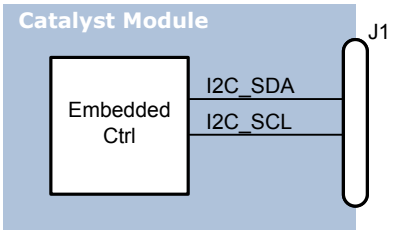
- MMC 4.0 specification allowing clock frequencies up to 48 MHz and bus widths of 1, 4, or 8 bits.
- SDIO 1.1 specification allowing clock frequencies up to 24 MHz and bus widths of 1 or 4 bits.

In addition to the SD/MMC signals, connector J1 includes signals to control SD/MMC support circuitry on the carrier board. Each interface includes signals to control a power FET and to drive a LED. See Design Constraints, page 27 for routing guidelines.

I²C Bus

I²C (Inter-IC) bus is a multi-master, "two-wire" synchronous serial bus for communications between integrated circuits (ICs) and for addressing peripherals in a system. Connector J1 includes an external connection to the I²C bus of the Catalyst Module embedded controller. This interface is intended for communication between the embedded controller and the temperature monitoring circuitry on the carrier board; however, it can be used to communicate with other I²C devices.

The following diagram illustrates the I²C architecture on the Catalyst Module. Notice that the Catalyst Module does not include termination on the I²C bus. Include 10kΩ pull-up resistors to V3.3A on the carrier board.

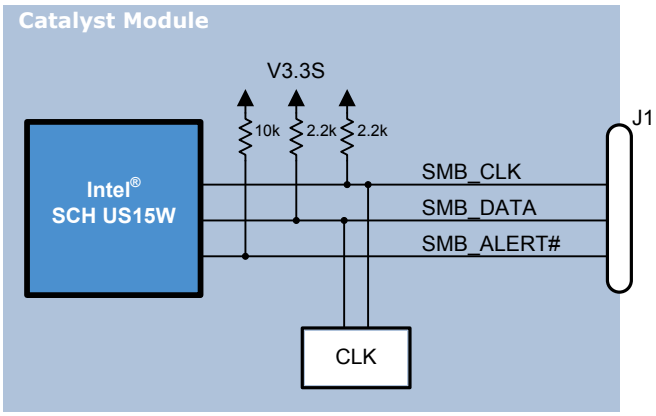


System Management Bus

System Management Bus (SMBus) follows the same operating principles as I²C. Similar to I²C, SMBus is a “two-wire” interface allowing multiple devices to communicate with each other. Devices function as bus masters and bus slaves. However, the SMBus specification defines electrical characteristics for the special needs of batteries. SMBus enables communication for power management related tasks and allows connection of devices that require legacy software accessibility thru standard SMB addressing. SMBus is not compatible with all I²C devices. Review the device data sheet carefully before connecting an I²C device to the SMBus.

Connector J1 includes an external connection to the Intel SCH US15W SMBus. Use this interface to communicate with devices on the carrier board. In addition, the Catalyst Module supports hardware alerting on the SMBus using the I/O signal SMB_ALERT#.

The following diagram illustrates the SMBus architecture on the Catalyst Module.



The following table lists the addresses of the SMBus devices on the Catalyst Module.

Module Device	Address	Function
Reserved	0101 0010	Write
	0101 0011	Read
Clock Generator	1101 0010	Write
	1101 0011	Read

User Interface and Display

The Intel SCH US15W includes an integrated 2D/3D graphics controller supporting hardware-accelerated graphics display and video processing capabilities. The controller provides two independent display interfaces. A 4-channel LVDS interface drives the primary display, while a Serial Digital Video Out (SDVO) interface drives a secondary display. In addition, the Catalyst Module provides discrete backlight control signals.

This section summarizes the Catalyst Module graphics display and video processing capabilities. Display resolutions are specified at the maximum refresh rate and color depth. The graphics display processing performance, as measured by refresh rate, is expected to be roughly inversely proportional to the display resolution and to the dual display output modes. Higher resolutions may be possible at lower refresh rates and color depths. This relationship is due primarily to the increased processing bandwidth required at higher output resolutions.

LVDS Display

The growing demand for higher resolution displays has been meet with design limitations on the interface between the LCD and graphics controller. Increased resolution LCDs require an increased clock speed, a larger number of data lines, and a higher power consumption. LVDS serial data transmission addresses these issues by providing a high-speed, low-power interface on a single pair of wires per channel. The Intel SCH US15W supplies a LVDS interface to drive a primary display.

The following table summarizes the LVDS display capabilities.

Feature	LVDS Display
Resolution	Single display up to 1366 x 768 at 85 Hz, 8-bit per lane or dual display up to 1280 x 768 at 85 Hz, 8-bit per lane
Configurations	Extended Display Identification Data (EDID) and non-EDID
Operation	Extended desktop or clone mode
Display parameter	Centering, scaling, and rotation

The LVDS display interface consists of four LVDS data pairs, as well as a LVDS pixel clock. These differential pairs require strict routing constraints on the carrier board. See Design Constraints, page 27 for routing guidelines.

Additional capabilities include the discrete signal L_VDDEN (J1 pin A32) that controls power to the display and two I^2C interfaces for communication with the LCD. One I^2C interface connects with the LCD DDC, while the other connects to the backlight.

SDVO Interface

In addition to the LVDS display interface, the Intel SCH US15W drives a secondary display on the SDVO interface. SDVO allows for an additional video interface using a PCIe x16 slot implemented on a carrier board. This secondary interface supports external devices that convert the SDVO protocol to DVI, HDMI, LVDS Analog-CRT, and TV-Out interfaces. Contact your local Eurotech technical support for recommended Intel/HP SDVO cards.

The following table summarizes the SDVO interface capabilities.

Feature	SDVO Interface
Resolution	Single display up to 1280 x 1024 at 85 Hz, full color or dual display up to 1280 x 768 at 85 Hz, full color
Configurations	EDID and non-EDID
Operation	Extended desktop or clone mode
Formats	DVI and HDMI formats with panning and device hot plug, LVDS formats with scaling, and TV-Out in NTSC, PAL and SECAM SD formats

The SDVO interface includes seven high-speed differential pair signals. Routing the high-speed differential pairs on the carrier boards requires strict design constraints. See Design Constraints, page 27 for routing guidelines.

In addition, the SDVO interface includes an I^2C bus. This bus connects to a SDVO panel DDC. The Catalyst Module does not include termination on the I^2C signals. Include 3.5KΩ pull-up resistors to +2.5V on the carrier board. If your carrier board does not generate +2.5V and your design does not use the SDVO I^2C signals, these signals can be pulled to V3.3S with 1MΩ resistors.

Backlight

Most LCDs include one or more cold-cathode fluorescent lamp (CCFL) tubes to backlight the displays. Backlight inverters drive the panel backlights. These circuits are typically external to the display and generate the several hundred volts required to drive the CCFL tubes. Backlights can easily become the greatest source of power consumption in a portable system.

To reduce power consumption, most backlight inverters include control signals to dim and turn off the backlight. To support these features, the Intel SCH US15W supplies three backlight control signals as described in the following table.

Signal	J1 Pin	Type	Description
L_BKLTCTL	B33	O-PWM	Controls the intensity of the backlight
L_BKLTEN	B32	O	Turns power to the backlight on or off
L_BKLTSEL	B58	O	Selects backlight control (PWM vs. I^2C)

Inputs and Outputs

Several signals support a modular architecture and provide I/O expansion. The Catalyst Module includes a Low Pin Count bus supporting legacy I/O capabilities and multiple discrete I/O signals performing system reset, system management, power control, and general-purpose input and output. Connector J1 includes all I/O signals.

Low Pin Count Bus

In response to the transition from ISA-based systems, the Low Pin Count (LPC) bus provides a migration path for legacy I/O capabilities. This interface enables general-purpose I/O expansion and provides communication to low-bandwidth devices. The Intel SCH US15W supplies a LPC bus for this purpose. On the Catalyst Module, the LPC bus connects to the embedded controller. While on the Catalyst Module XL, this bus connects to the embedded controller and optional TPM. Externally, the LPC bus provides general-purpose expansion. Common applications on the carrier board include an external BIOS option and a Super I/O Controller that provides I/O capabilities such as serial ports, keyboard, mouse, IrDA, and general-purpose I/O.

An additional signal, LPCPD# (J1 pin B2), is driven by the embedded controller indicating an in-process system power state change to attached LPC bus devices. When this signal is active, the attached peripherals should prepare for a power down event. See Electrical, page 46 for further details.

Ensure that the LPC signals are routed as critical nets on the carrier board. See Design Constraints, page 27 for routing guidelines. Include 10kΩ pull-up resistors to V3.3S on the LPC_ADx signals.

Reset Signals

One of two signals resets the circuitry on the module and carrier board. One signal originates from the module, while the second signal originates from the carrier board. The output signal RESET# includes several loads on the Catalyst Module. Include a buffer on the carrier board to drive additional loads.

The following table compares the reset signals.

Signal	J1 Pin	Type	Description
RESET#	B56	O	Output is driven by the module, forces complete system hardware reset, and is used for proper reset timing and logic synchronization.
FP_RESET#	A59	I	Input connects to a button on the carrier board and initiates a hardware reset including the Intel Atom processor and Intel SCH US15W.

In addition to the hardware resets, the input signal H_INIT# (J1 pin B3) initiates a soft reset of the module. See Electrical, page 46 for further details.

System Management

The signal THERM_ALERT (J1 pin A109) performs two system management functions as described in the next table. This signal interfaces with the embedded controller and is programmable. See Electrical, page 46 for further details.

State	Type	Description
Normal operation	O	High indicates detection of a thermal “over-temperature” event.
System reset	I	Low for a minimum of 200ns immediately preceding de-assertion of system reset signal enables the external BIOS option.

General-Purpose Input and Output

The embedded controller supplies two general-purpose input and output (GPIO) signals. See Electrical, page 46 for further details.

Intel High Definition Audio

The Intel High Definition Audio (Intel HD Audio) specification implements high quality audio in a PC environment. The specification defines a uniform interface between a host computer and audio codec specifying register control, physical connectivity, programming model, and codec architectural components. The Intel SCH US15W includes an Intel HD Audio interface capable of supporting up to two external audio codecs. The audio codecs along with amplifiers and switches are located on the carrier board. Docking functionality is supported allowing control of an external switch for isolation of the codec within a docking station during normal docking request and acknowledge cycles.

All Intel HD Audio signals are available on connector J1. See Electrical, page 46 for the Intel HD Audio electrical specification and see Design Constraints, page 27 for routing guidelines. The interface supports 3.3 V or 1.5 V signaling levels. Standard Catalyst Modules support 3.3 V signaling levels. Contact your local Eurotech technical support if your application requires 1.5 V.

Power Requirements

Power management is especially critical in high-performance systems that also require low power dissipation. Handheld and portable systems available today never really turn "off". They make use of power management techniques that cycle the electronics into power saving modes, but never fully remove power from the full system. This section provides information about power and power management on the Catalyst Module.

Low Power States

The Catalyst Module supports the Advanced Configuration and Power Interface (ACPI) specification. Unlike previous power standards that were BIOS-based, ACPI allows OS-directed power management. It specifies an industry-standard interface for both hardware and software that facilitates power and thermal management. This section describes how the Catalyst Module makes use of the ACPI low power modes.

Embedded system designers using the Catalyst Module should have a clear understanding of how the system design allocates power usage. Create a power budget that takes into account the types of devices that are used with the Catalyst Module. See Power, page 44 for baseline power consumption for the module.

The ACPI specification defines the low power states for ACPI-compliant systems. The following table describes the states supported by the Catalyst Module.

State	Mode	Description
S0	Full Operation	All devices are operational with dynamic power management functions active.
S3	Standby or Sleep	The Intel Atom processor and Intel SCH US15W are powered down. Active operating system context stored in DRAM is retained using low-power self-refresh. Wake events are active and enable a transition back to full operation.
S4	Hibernation	The Intel Atom processor, Intel SCH US15W, DRAM, and embedded controller are powered down. Operating system context is saved to disk storage prior to powering down system voltage rails. Limited wake events are active. Resume to full operation is dependent on numerous system components including the disk storage device.
S5	Power down	The Intel Atom processor, Intel SCH US15W, and DRAM are powered down. The embedded controller is active but may be in low-power mode. No operating system context is preserved. Limited wake events are active.

Wake events transition the Catalyst Module from a low-power state back to full operation. The following table lists the signals that can function as wake events.

Wake Event	J1 Pin	Description
FWH_WP#	A2	Wake event when programmed as GPIO
SMB_ALERT#	A33	SMBus activity alert
USB_CLIENT	B53	USB2 client detection when programmed as GPIO
PCIE_WAKE#	B55	Standard I/O device wake event signal
L_BKLTSEL	B58	Wake event when programmed as GPIO

Power Supply Architecture

The architecture of the power supply partitions the power generation across the Catalyst Module and the carrier board. The module requires 5 V and 3.3 V input voltages supplied by the carrier board. It is the responsibility of the carrier board designers to provide input power protection as required by their application. This is especially important if the power supply wires will be subject to EMI/RFI or ESD. On-module regulators generate the core power and all other powers required by the supporting circuitry.

See Power, page 44 for further details.

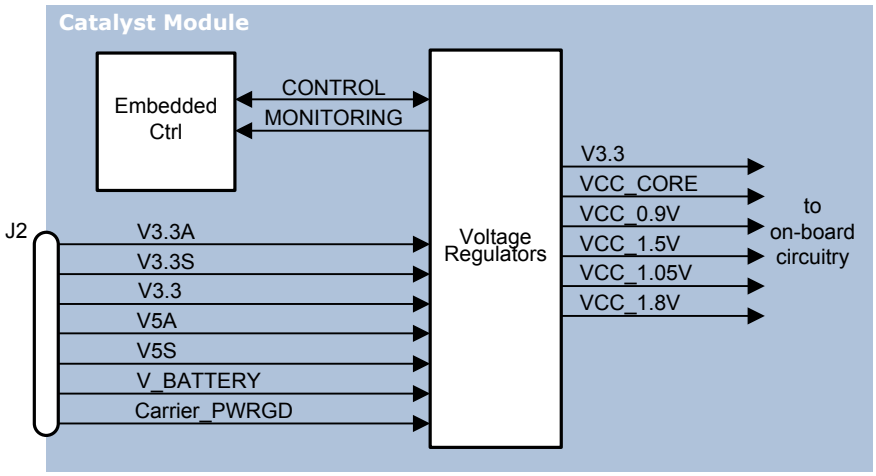
Input Power Voltages

The following table describes the input power voltages required by the Catalyst Module.

Name	Power State	Description
V3.3	S0 operation and S3 operation	3.3 V primary supply voltage for most of the on-board regulated voltages
V3.3S	S0 operation	3.3 V normal operating power
V5S	S0 operation	5 V normal operating power
V3.3A	S4 exit, S5 exit, S0 operation, and S3 operation	3.3 V “always” power for up/down circuitry only
V5A	S4 exit, S5 exit, S0 operation, and S3 operation	5 V “always” power for up/down circuitry only
V_BATTERY		Backup power for the RTC

The embedded controller controls proper sequencing of voltages to allow for proper start-up, shutdown, and power saving transitions. In addition, it monitors input power voltages and the on-module voltage regulators.

The following diagram illustrates the layout of the Catalyst Module power supply. Notice that voltages ending with an “A” indicate supplies that are always on, while voltages ending with an “S” indicate supplies that are switchable.



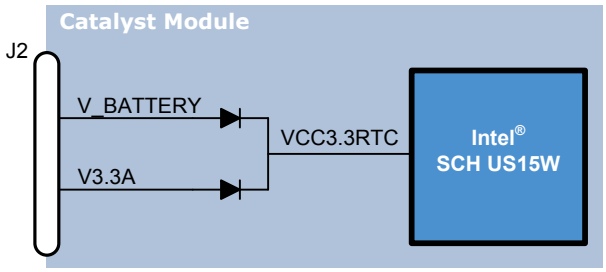
Note: The V5A rail should lead the V3.3A rail during ramp up or not lag by more than 0.7 V. The V5S rail should lead the V3.3S rail during ramp up or not lag by more than 0.7 V.

In addition to the input power voltages, connector J2 includes the signal Carrier_PWRGD. This input from the carrier board indicates that all input power voltages are fully operational and within tolerance. The carrier board must provide this signal to represent the readiness for operation.

RTC Backup Power

The Catalyst Module includes a RTC function that retains the system date and time when the system is powered down as long as the 3.3 V “always” power or backup power is provided to the module. Including a long-life 3 V battery on a carrier board is a common method to supply backup power. Use series elements, such as a diode and resistor, on the V_BATTERY output from your carrier board based on your specific requirements.

The V_BATTERY power input has a diode-OR with V3.3A on the Catalyst Module as shown in the following diagram.



See Power, page 44 and General, page 48 for further details.

Power Switch

The input signal PWR_BUTTON# (J1 pin B59) controls a power switch included on the Catalyst Module. An external momentary button connected to this signal turns module power on and off. See Electrical, page 46 for further details.

The following table details the operation of the PWR_BUTTON# signal.

State	Operation
Power off	Momentary assertion initiates a power up sequence.
Power on (default)	Momentary assertion initiates an orderly shutdown sequence and power-off.
Power on (options)	Momentary assertion initiates system sleep states, or continuous assertion (4 second minimum) initiates a power-off-over-ride sequence and immediate power-off.

The result of the PWR_BUTTON# signal is operating system dependent. Pressing the external momentary button in DOS will turn the power off; however, the result could be an S3 with a different operating system.

Note: Once the V5A and V3.3A rails are applied, the PWR_BUTTON# signal is not detected for 400 msec.

Power State Signals

The Catalyst Module provides three control signals on connector J1 indicating the power state. The embedded controller drives the two power state signals, PM_EN_S0# (J1 pin B104) and PM_EN_S3# (J1 pin B107). The on-module power switch controls the remaining signal, PM_EN_PWR (J1 pin B105). See Electrical, page 46 for further details.

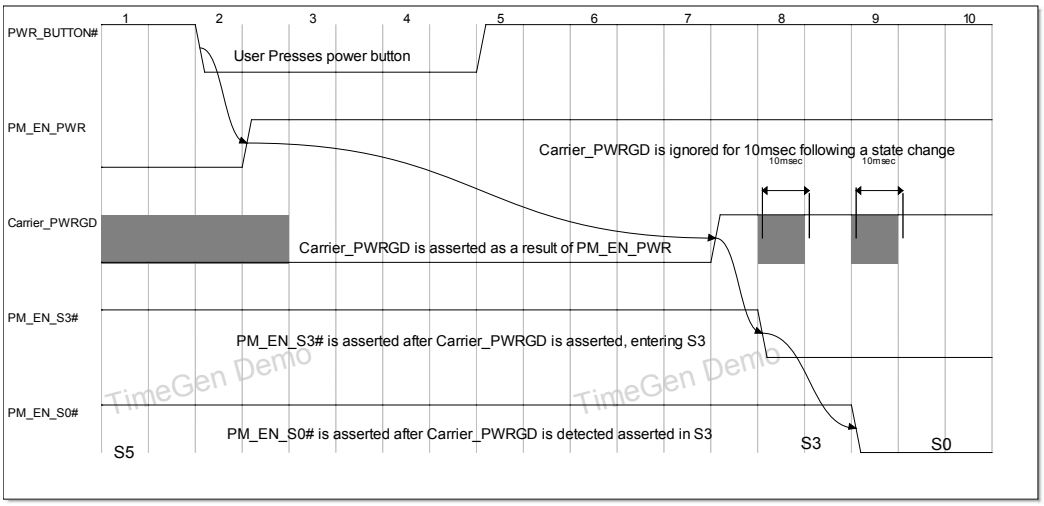
The next table lists these signals with the power states and input power voltages active in each state.

State	Active power rails	Power State Signals		
		PM_EN_PWR	PM_EN_S3#	PM_EN_S0#
S0	V3.3, V5S V3.3S V5A, V3.3A	High	Low	Low
S3	V3.3, V5A, V3.3A	High	Low	High
S4	V5A, V3.3A	Low	High	High
S5	V5A, V3.3A	Low	High	High

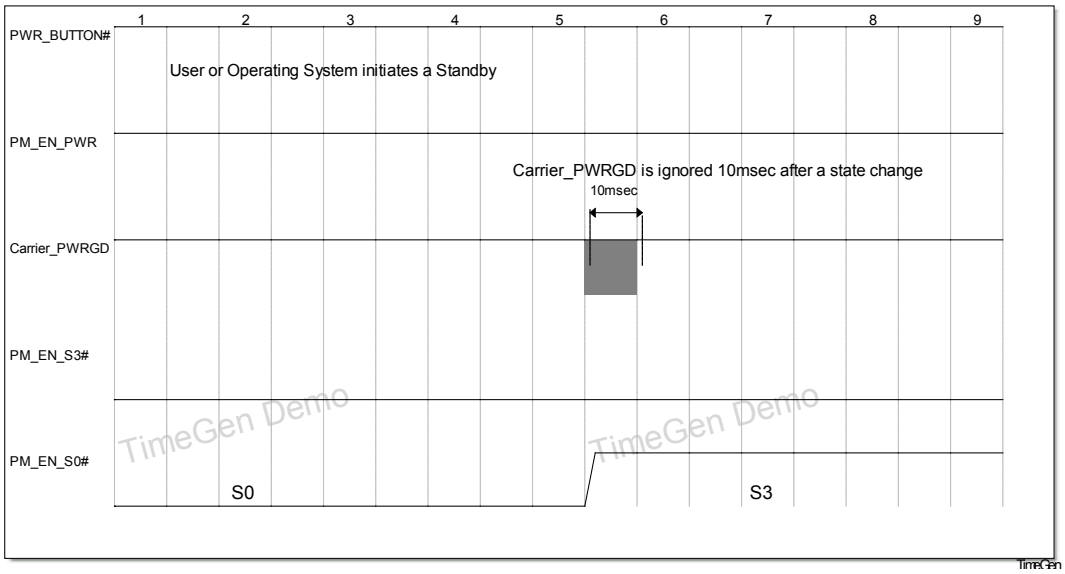
This section includes timing diagrams that describe the relationship of the power state control signals on the Catalyst Module.

In a typical system power on, the falling edge of PWR_BUTTON# drives PM_EN_PWR low. A hardware latch on the Catalyst Module controls PM_EN_PWR. The embedded controller monitors PWR_BUTTON# until the rising edge of PWR_BUTTON#. After sampling PWR_BUTTON# high, the embedded controller waits for Carrier_PWRGD to be asserted high before driving PM_EN_S3# active (logic level low). S3 power rails internal to the Catalyst Module are enabled with the assertion of PM_EN_S3# and powered by V3.3. After the S3 power rails are within specification, the embedded controller asserts PM_EN_S0# (logic level low). The time from PM_EN_S3# active to PM_EN_S0# active depends on how quickly the carrier supplies V3.3. Typically, the Catalyst Module transitions from S3 to S0 within 50msec.

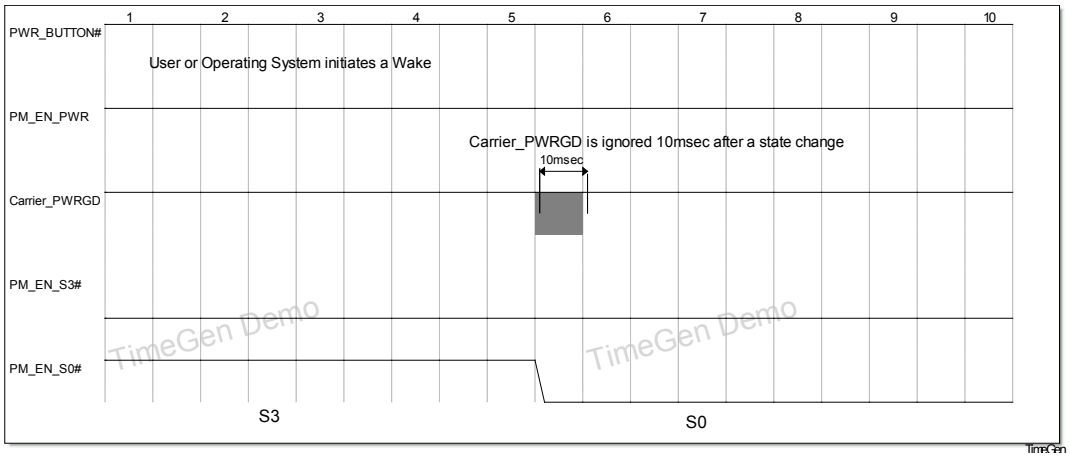
Power on initiated by power button press



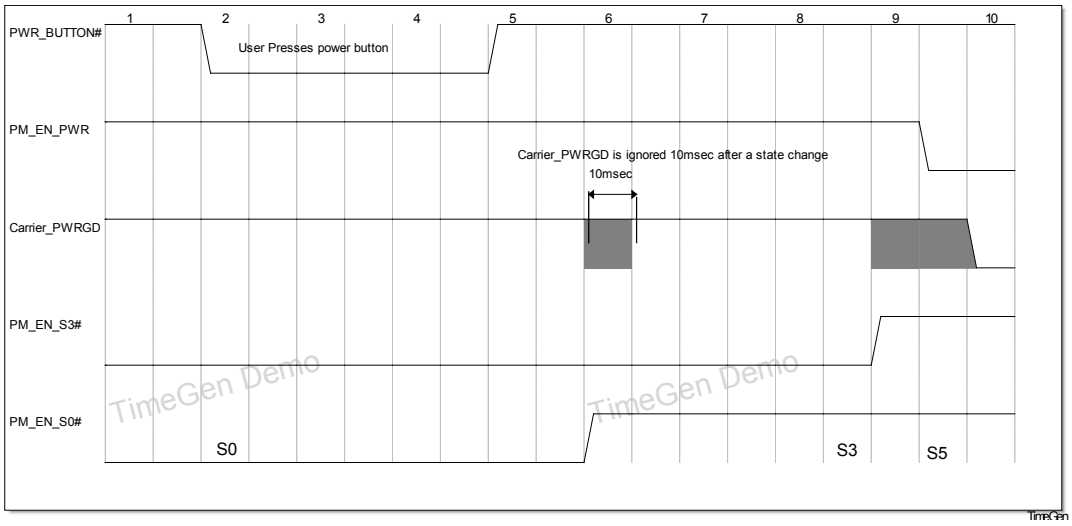
Standby (Enter S3)



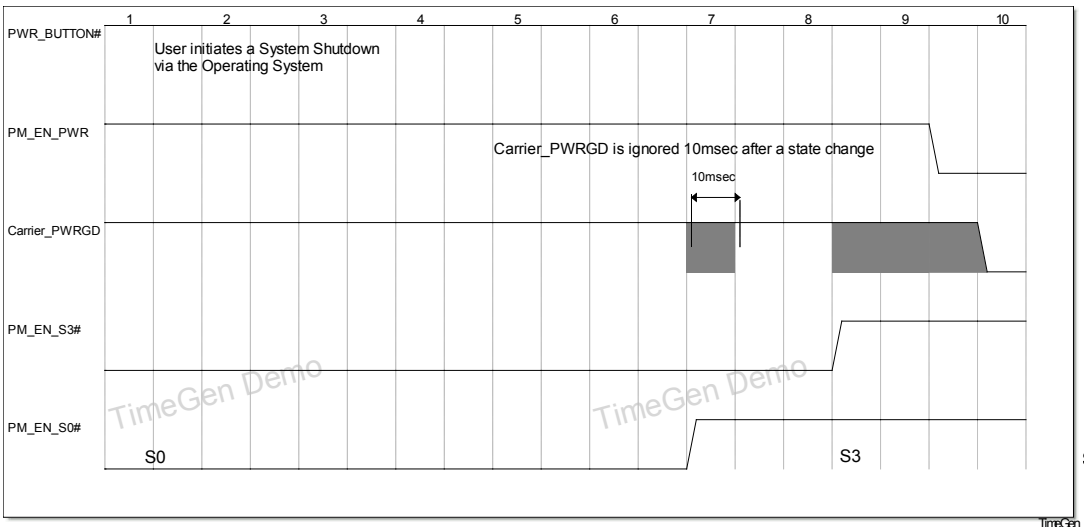
Standby (Exit S3)



Power off initiated by power button press



System shutdown initiated by operating system



Carrier Board Design

An application-specific carrier board integrates with the Catalyst Module to meet various system requirements. The Catalyst Module Development Kit includes a carrier board designed to maximize the Catalyst Module functionality. This carrier board implements many industry-standard interfaces and provides a reference for custom carrier boards optimized for your requirements. This section includes many of the considerations followed in the design of the Catalyst Module and carrier board.

Design Constraints

Increasing reliability is a key consideration in the Catalyst Module design. Several constraints followed in the module design and printed wiring board (PWB) layout ensure superior product reliability and compatibility. Use similar constraints in the carrier board design.

The following are the design considerations used to improve the Catalyst Module reliability:

- Advanced high-speed signal routing techniques
  - Strict adherence to signal routing rules as collaborated with Intel design and simulation teams
    - Minimum and maximum trace lengths
    - Total, segment, and multi-segment including package length compensation
    - Bus and group length matching to +/- 1mil
    - Continuous trace matching for differential pair routing
  - Impedance matching and controlled design
    - 50% de-rating design constraint for guaranteed margin in high volume production
    - Consideration of I/O buffer characteristic variances over extended temperature ranges for improved electrical performance
    - 100% continuous ground return path for all high-speed signals
    - Routing over continuous planes for consistent transmission line impedance and clean, reliable signal transitions
- Conservative level 4 printed wiring design construction
  - Durable feature sizes and construction elements
    - Pads, fills, and holes optimized for ROHS processing and long term reliability
  - Buried power planes between ground layers to eliminate coupling with high-speed signals
  - De-rating for current loading on the power regulation circuit and interface
  - No bottom side “hot” power regulation components underneath the Intel Atom processor or the Intel SCH US15W that would reduce thermal performance

EMI/RFI Protection

Many products using Eurotech single-board computers have successfully completed FCC and CE emissions testing as a part of their design cycle. The Catalyst Module incorporates the following design considerations that reduce emission and improve immunity:

- Four extra solid ground planes
- High-speed signal routing on internal ground referenced layers
- No high-speed signal return currents passed thru coupling capacitors
- EMI ring on module perimeter

Routing Guidelines

Proper signal routing is critical to a successful carrier board design. The Catalyst Module supports high-speed differential and single-ended signals that require strict routing constraints.

Use the following recommendations to route high-speed signals:

- Ground references
- Continuous reference planes
- Matched lengths
- Bend minimization
- Layer-to-layer connection reduction

Contact your local Eurotech technical support for additional signal routing details.

The following are the high-speed differential pairs that require strict routing constraints on a carrier board:

- USB
  These signal pairs can be routed to USB sockets for external connections or directly to USB devices on the carrier board. Include an EMI choke between connector J1 and the USB connector when driving a USB cable. Applications with USB devices hardwired on-board do not require an EMI choke.
- PCIe
  Each PCIe x1 bus consists of differential signal pairs for transmit (PET), receive (PER), and reference clock (REFCLK). The module includes AC coupling capacitors on the PET pair. Include AC coupling capacitors on the PER pair driven from the carrier board to the Catalyst Module. The recommended coupling capacitor is a 0.1μF surface mount 0402 discrete capacitor of type X7R/X5R.
- LVDS display
  The LVDS display interface includes four LVDS data pairs and a LVDS pixel clock.
- SDVO Interface
  The SDVO interface consists of seven high-speed differential signal pairs.

The following are the high-speed single-ended signals that require strict routing constraints on a carrier board:

- IDE/PATA interface
- HD Audio
- SD/MMC
- LPC bus

Requirements and Recommendations

The previous sections provided details about the various features of the Catalyst Module including design requirements and design recommendations. This section summarizes these design guidelines and provides a checklist for custom carrier board design.

The following table lists circuitry required on the carrier board.

Name	Pin	Carrier Board Design Requirement
PM_EN_S3#	J1 B107	Include 10kΩ pull up resistor to V3.3A
FP_RESET#	J1 A59	Include momentary button
PWR_BUTTON#	J1 B59	Include momentary button
USB_CLIENT	J1 B53	Include 4.7kΩ pull up resistor to 3.3 V
PCIE1_PER+ PCIE1_PER-	J1 B95 J1 B94	Include 0.1µF AC coupling capacitors
PCIE2_PER+ PCIE2_PER-	J1 A95 J1 A94	Include 0.1µF AC coupling capacitors
V_BATTERY	J2 4	Include 3 V battery
SDVO_CLK+ SDVO_CLK-	J1 B91 J1 B92	Include 0.1µF AC coupling capacitors Include 0.1µF AC coupling capacitors

The following table lists recommendations for circuitry on the carrier board.

Name	J1 Pin	Carrier Board Design Recommendation
TDO	A106	Include 10kΩ pull-up to V3.3S
CLK_LPC_FWH	A36	Include no more than one load
CLK_LPC_SIO	B37	Connect to legacy IO controller if required
SDVO_CTLCLK SDVO_CTLDATA	B30 A30	Include 3.5K Ω pull-up to 2.5V Include 3.5K Ω pull-up to 2.5V
LPC_AD3 LPC_AD2 LPC_AD1 LPC_AD0	B38 B34 B39 B36	Include 10kΩ pull-up to V3.3S Include 10kΩ pull-up to V3.3S Include 10kΩ pull-up to V3.3S Include 10kΩ pull-up to V3.3S
RESET#	B56	Buffer for signal drive strength
I2C_SDA I2C_SCL	B108 B109	Include 10kΩ pull-up to V3.3A
L_DDC_CLK L_DDC_DATA	A 29 B 28	Include a 10kΩ pull up to V3.3S Include a 10kΩ pull up to V3.3S
L_BKLTEN	B 32	Include a 100kΩ pull down

Name	J1 Pin	Carrier Board Design Recommendation
L_CTLA_CLK	B 29	Include 4.7kΩ pull up to V3.3S
L_CTLB_DATA	B 25	Include 4.7kΩ pull up to V3.3S
L_VDDEN	A 32	Include a 100kΩ pull down
SD0_WP	B 12	Include a 10kΩ pull up to V3.3S
SD1_WP	B 16	Include a 10kΩ pull up to V3.3S
SD2_WP	B 27	Include a 10kΩ pull up to V3.3S
THERM_ALERT	A109	Can be un-connected if unused
USB0+	A71	Include an EMI choke between connector J1
USB0-	A72	and the USB connector
USB1+	B71	Include an EMI choke between connector J1
USB1-	B72	and the USB connector
USB2+	A68	Include an EMI choke between connector J1
USB2-	A69	and the USB connector
USB3+	B67	Include an EMI choke between connector J1
USB3-	B68	and the USB connector
USB4+	A65	Include an EMI choke between connector J1
USB4-	A66	and the USB connector
USB5+	B64	Include an EMI choke between connector J1
USB5-	B65	and the USB connector
USB6+	A62	Include an EMI choke between connector J1
USB6-	A63	and the USB connector
USB7+	B61	Include an EMI choke between connector J1
USB7-	B62	and the USB connector

Test and Debug

The Catalyst Module provides the required signals on connector J1 to support a full IEEE1149.1 JTAG port and a maintenance port for the embedded controller. These interfaces are available for factory test and for board-level software debugging; otherwise, the ports are not supported for application use. To ensure correct operation of the JTAG interface, include a 10kΩ pull-up resistor to V3.3S on the TDO signal on the carrier board.

An additional ITP debug port, connector J3, provides full access to the XDP debugger port using a SFF style connector.

Mechanical

The Catalyst Module is 100 mm by 67 mm in size. This section describes the component dimensions and mounting of the board.

Mounting Holes

Four holes enable mounting on the carrier board. Along one side, two mounting holes are located on each corner. The mounting holes are placed off set from the corners along the opposite side of the module.

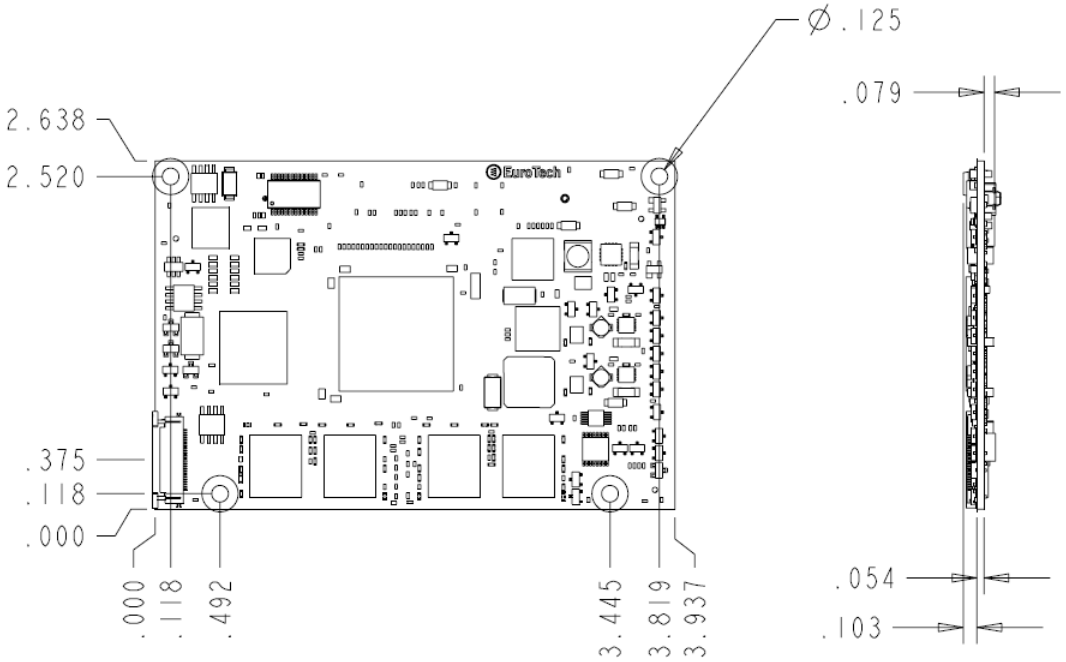
The Catalyst Module ground plane connects electrically to the mounting holes. For reliable ground connections, use locking washers when securing a module to a carrier board. Make sure that washers do not extend beyond the limits of the pads provided.

Mechanical Drawing

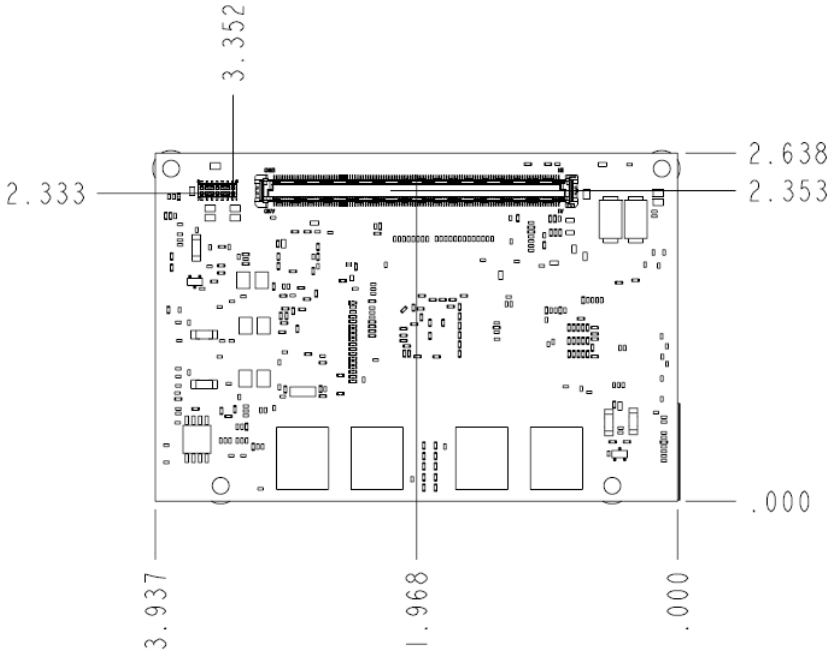
Catalyst Module

The following mechanical drawing specifies the dimensions of the Catalyst Module, as well as locations of key components on the board. All dimensions are in inches.

The first diagram illustrates the component and side views of the module.



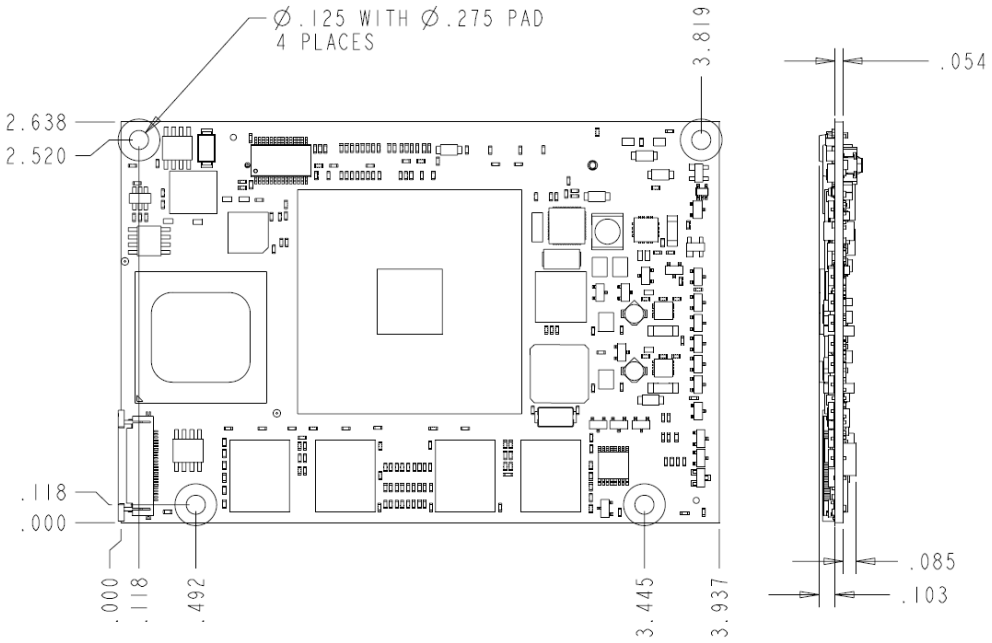
The next diagram illustrates the underside of the module. Notice connector J1 and J2 are located on the underside.



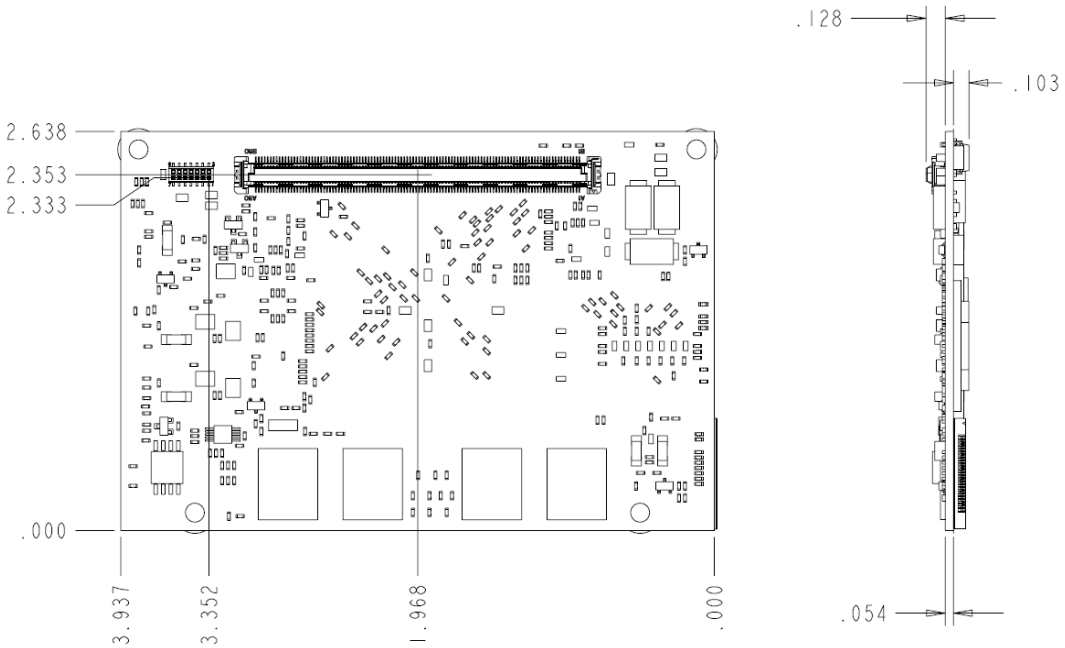
Catalyst Module XL

The following mechanical drawing specifies the dimensions of the Catalyst Module XL, as well as locations of key components on the board. All dimensions are in inches.

The first diagram illustrates the component and side views of the module.



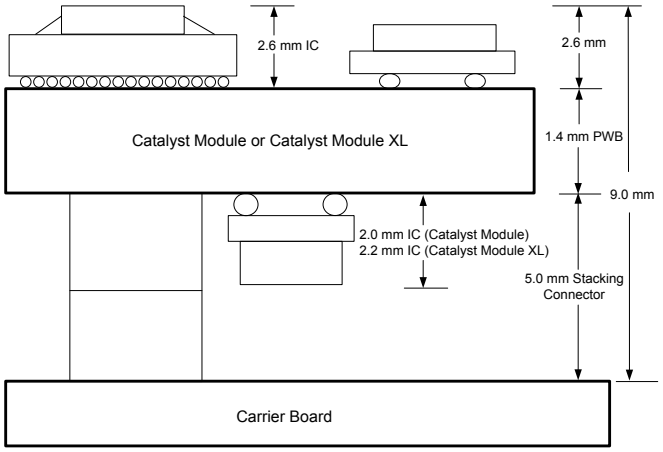
The next diagram illustrates the bottom and side views of the module. Notice connector J1 and J2 are located on the underside.



Total Stack Height

Selection of low profile stacking connectors and components minimizes the total stack height of the Catalyst Module and carrier board. The module uses stacking board-to-board connectors to mate with a carrier board. The mating connectors on the carrier board can be either 5 mm or 8 mm stacking height. When 5 mm stacking board-to-board connectors are used, the total board height combined with the connector clearance results in a total stack height of less than 10 mm. You may place components under the module on a custom carrier board. However, the design must allow adequate heat dissipation.

The following diagram illustrates the total stack height using 5 mm stacking connectors on the carrier board.



Installing and Removing the Catalyst Module

The Catalyst Module connects to the carrier board through two connectors that are in line with each other. A high-density, stacking board-to-board connector carries the data signals, while a smaller 2x7-pin 1 mm-pitch connector carries power. When fully connected, these fine pitch connectors provide reliable and durable connection. However, care is required when removing or installing the module onto the carrier board. If correct procedures for installation and removal are not followed, damage to the connectors and/or the connector pins can result.

For detailed procedures to install a module onto or remove a module from a carrier board, refer to the Catalyst Module Installation and Removal Technical Support Bulletin (Eurotech document 110122-2014).

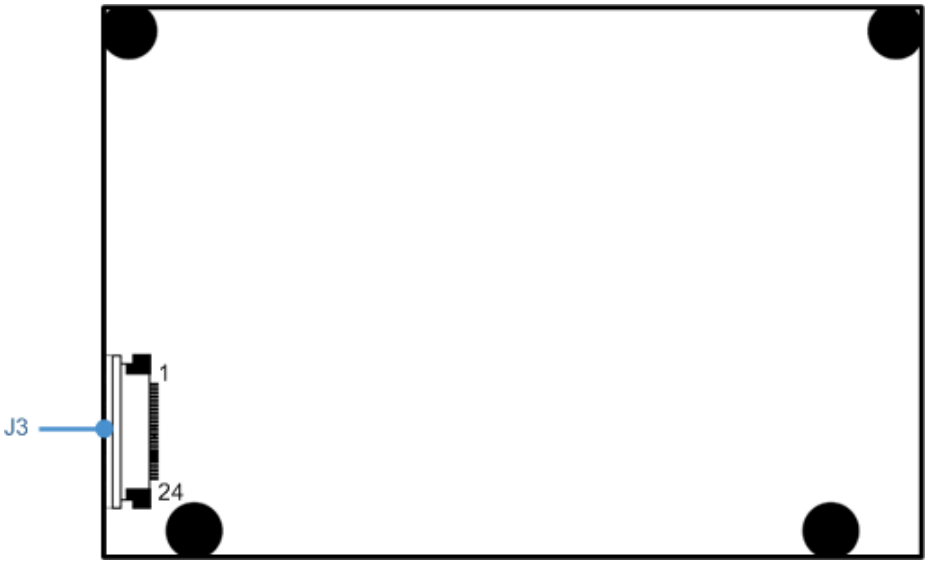
Important! Observe industry-standard electronic handling procedures when handling the module. The connectors expose signals on the system bus that do not have ESD protection.

Connectors, LEDs, and Jumpers

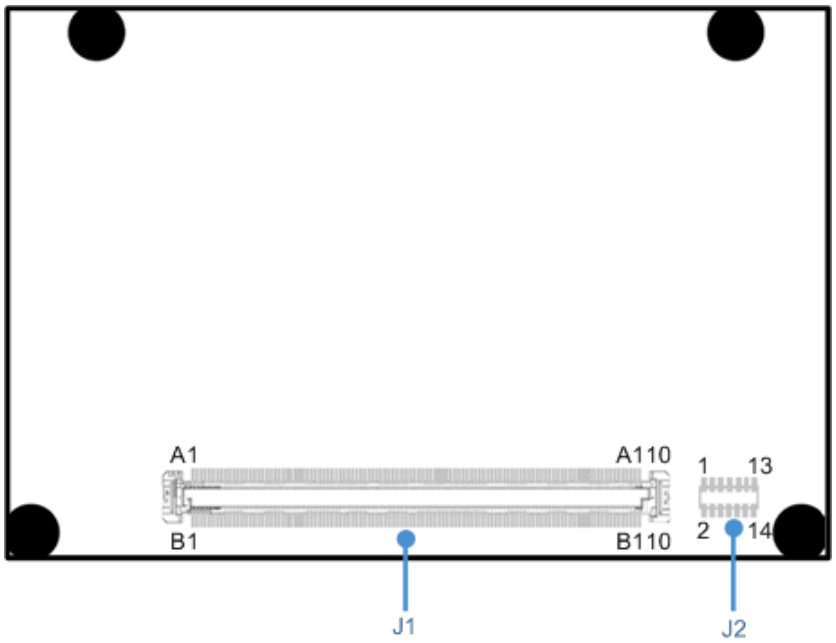
Identifying Connectors

The following diagrams illustrate the location and numbering of the connectors on the Catalyst Module. When viewing the module from the component side, connector J1 and connector J2 lie under the module.

The first diagram illustrates the component side of the module.



The second diagram illustrates the underside of the module.



Signal Headers

The following tables describe the electrical signals available on the connectors of the module. Each section provides relevant details about the connector including part numbers, mating connectors, signal descriptions, and references to related sections.

J1: Docking Connector: Data

Board connector: 220-pin, stacking board-to-board receptacle, 0.5 mm, Tyco Electronics 3-6318490-6

Carrier board connector: Tyco Electronics 3-1827253-6, 5 mm stacking height
Tyco Electronics 3-6318491-6, 8 mm stacking height

The Catalyst Module connector J1 mates to the carrier board. Most data signals are provided on this docking connector.

Pin	Name	Type	On Module Termination	Description
A1	GND	P		Ground
A2	FWH_WP#	O-CMOS		External BIOS option write protect
A3	GPIO2	IO-CMOS		GPIO
A4	HDA_SYNC	O-HDA		Intel HD Audio
A5	HDA_RST#	O- HDA		
A6	HDA_SDI0	I- HDA		
A7	HDA_SDI1	I- HDA		
A8	reserved			
A9	SD0_DATA3	IO-LVTTL	R 48Ω	SD/MMC0
A10	SD0_DATA1	IO-LVTTL	R 48Ω	
A11	GND	P		Ground
A12	SD0_LED	O-LVTTL		SD/MMC0
A13	SD0_CLK	O-LVTTL	R 48Ω	
A14	SD1_DATA1	IO-LVTTL	R 48Ω	SD/MMC1
A15	reserved			
A16	SD0_PWR#	O-LVTTL		SD/MMC0
A17	SD1_PWR#	O-LVTTL		SD/MMC1
A18	SD1_LED	O-LVTTL		
A19	SD1_CLK	O-LVTTL	R 48Ω	
A20	SD1_CD#	I-LVTTL	PU 10kΩ V3.3S	
A21	GND	P		Ground

Pin	Name	Type	On Module Termination	Description
A22	SD2_DATA3	IO-LVTTL	R 48Ω	SD/MMC2
A23	SD2_DATA5	IO-LVTTL	R 48Ω	
A24	SD2_LED	O-LVTTL		
A25	SD2_DATA7	IO-LVTTL	R 48Ω	
A26	SD2_DATA1	IO-LVTTL	R 48Ω	
A27	SD2_DATA6	IO-LVTTL	R 48Ω	
A28	SD2_CLK	O-LVTTL	R 48Ω	
A29	L_DDC_CLK	O-LVTTL		LCD DDC I^2C
A30	SDVO_CTLDATA	IO		SDVO DDC I^2C
A31	GND	P		Ground
A32	L_VDDEN	O-LVTTL		LCD power enable
A33	SMB_ALERT#	OD-LVTTL	PU 10kΩ V3.3S	SMBus activity alert
A34	HDA_SPKR	O-HDA		Intel HD Audio
A35	LPC_CLKRUN#	IO-LVTTL	PU 8.25kΩ V3.3S	LPC bus
A36	CLK_LPC_FWH	O-LVTTL	R 22Ω	LPC bus or External BIOS option clock
A37	IDE_DIOW#	O-LVTTL		IDE/PATA interface
A38	SMB_CLK	OD-LVTTL	PU 2.2kΩ V3.3S	SMBus clock
A39	LPC_SERIRQ	OD-LVTTL	PU 10kΩ V3.3S	LPC bus
A40	LPC_FRAME#	O-LVTTL		
A41	GND	P		Ground
A42	IDE_A00	O-LVTTL		IDE/PATA interface
A43	IDE_DATA00	IO-IDE		
A44	IDE_DATA03	IO-IDE		
A45	IDE_DATA09	IO-IDE		
A46	IDE_A02	O-LVTTL		
A47	IDE_DATA05	IO-IDE		
A48	IDE_DATA06	IO-IDE		
A49	IDE_DATA01	IO-IDE		
A50	IDE_IOR#	O-LVTTL		
A51	GND	P		Ground
A52	IDE_DATA02	IO-IDE		IDE/PATA interface
A53	IDE_IRQ	I-LVTTL	PU 10kΩ V3.3S	
A54	IDE_IORDY	I-LVTTL	PU 4.7kΩ V3.3S	
A55	IDE_CS1#	O-LVTTL		
A56	IDE_CS3#	O-LVTTL		

Pin	Name	Type	On Module Termination	Description
A57	HDA_DOCK_EN#	O-HDA		Intel HD Audio
A58	HDA_DOCK_RST#	O-HDA		
A59	FP_RESET#	OD-3.3	PU 10kΩ V3.3S	Front panel reset
A60	GND	P		Ground
A61	USB_OC5#	I-LVTTL	PU 10kΩ V3.3	USB5 over current
A62	USB6+	IO		USB6 (high speed only)
A63	USB6-			
A64	GND	P		Ground
A65	USB4+	IO		USB4
A66	USB4-			
A67	GND	P		Ground
A68	USB2+	IO		USB2
A69	USB2-			
A70	GND	P		Ground
A71	USB0+	IO		USB0
A72	USB0-			
A73	GND	P		Ground
A74	LVDS_CLK+	O-LVDS		LVDS clock
A75	LVDS_CLK-			
A76	GND	P		Ground
A77	LVDS_DATA2+	O-LVDS		LVDS data 2
A78	LVDS_DATA2-			
A79	USB_OC2#	I-LVTTL	PU 10kΩ V3.3	USB2 over current
A80	GND	P		Ground
A81	LVDS_DATA1+	O-LVDS		LVDS data 1
A82	LVDS_DATA1-			
A83	GND	P		Ground
A84	SDVO_STALL+	I		SDVO signal allowing external device to stall the display pipeline
A85	SDVO_STALL-			
A86	GND	P		Ground
A87	SDVO_BLUE+	O	C 0.1µF	SDVO data
A88	SDVO_BLUE-			
A89	USB_OC3#	I-LVTTL	PU 10kΩ V3.3	USB3 over current
A90	GND	P		Ground

Pin	Name	Type	On Module Termination	Description
A91	SDVO_INT+	I		SDVO interrupt
A92	SDVO_INT-			
A93	GND	P		Ground
A94	PCIE2_PER-	I-PCIe		PCIe2 receive pair
A95	PCIE2_PER+			
A96	GND	P		Ground
A97	PCIE1_CLKREQ#	I-3.3	R 475Ω PU 10kΩ V3.3S	PCIe1 clock enable
A98	PCIE1_PET-	O-PCIe	C 0.1µF	PCIe1 transmit pair
A99	PCIE1_PET+			
A100	GND	P		Ground
A101	PCIE1_REFCLK+	O-HCSL		PCIe1 clock
A102	PCIE1_REFCLK-			
A103	GND	P		Ground
A104	TMS	O	PU 10kΩ V3.3S	JTAG
A105	TCK	I	PD 1kΩ	
A106	TDO	O		
A107	TDI	I	PU 10kΩ V3.3S	
A108	GPIO1	IO-CMOS		GPIO
A109	THERM_ALERT	IO-3.3	PU 10kΩ V3.3S	Thermal alert
A110	GND	P		Ground
B1	GND	P		Ground
B2	LPCPD#	O-3.3		In-process system power state change indicator
B3	H_INIT#	OD-LVCMOS	PU 1kΩ V1.05S	Soft reset for host processor
B4	HDA_CLK	O-HDA		Intel HD Audio
B5	HDA_SDO	O-HDA		
B6	SD0_CMD	IO-LVTTL	R 48Ω PU 40kΩ V3.3S	SD/MMC0
B7	SD0_DATA0	IO-LVTTL	R 48Ω	
B8	reserved			
B9	reserved			
B10	SD0_DATA2	IO-LVTTL	R 48Ω	SD/MMC0
B11	GND	P		Ground
B12	SD0_WP	I-LVTTL		SD/MMC0
B13	SD0_CD#	I-LVTTL	PU 10kΩ V3.3S	
B14	SD2_PWR#	O-LVTTL		SD/MMC2

Pin	Name	Type	On Module Termination	Description
B15	SD1_CMD	IO-LVTTL	R 48Ω PU 40kΩ V3.3S	SD/MMC1
B16	SD1_WP	I-LVTTL		
B17	SD1_DATA2	IO-LVTTL	R 48Ω	
B18	SD1_DATA0	IO-LVTTL	R 48Ω	
B19	SD1_DATA3	IO-LVTTL	R 48Ω	
B20	SD2_DATA0	IO-LVTTL	R 48Ω	SD/MMC2
B21	GND	P		Ground
B22	SD2_CD#	I-LVTTL	PU 10kΩ V3.3S	SD/MMC2
B23	SD2_DATA4	IO-LVTTL	R 48Ω	
B24	SD2_CMD	I-LVTTL	R 48Ω PU 40kΩ V3.3S	
B25	L_CTLB_DATA	IO-LVTTL		Backlight I^2C data
B26	SD2_DATA2	IO-LVTTL	R 48Ω	SD/MMC2
B27	SD2_WP	I-LVTTL		
B28	L_DDC_DATA	IO-LVTTL		LCD DDC I^2C
B29	L_CTLA_CLK	O-LVTTL		Backlight I^2C clock
B30	SDVO_CTLCLK	O		SDVO DDC I^2C
B31	GND	P		Ground
B32	L_BKLTEN	O		Turns power to the backlight on or off
B33	L_BKLTCTL	O-PWM		Controls intensity of the backlight
B34	LPC_AD2	IO-LVTTL	PU 10kΩ V3.3S	LPC bus
B35	SMB_DATA	IO-LVTTL	PU 2.2kΩ V3.3S	SMBus
B36	LPC_AD0	IO-LVTTL	PU 10kΩ V3.3S	LPC bus
B37	CLK_LPC_SIO	O-LVTTL	R 22Ω	
B38	LPC_AD3	IO-LVTTL	PU 10kΩ V3.3S	
B39	LPC_AD1	IO-LVTTL	PU 10kΩ V3.3S	
B40	IDE_DATA07	IO-IDE		IDE/PATA interface
B41	GND	P		Ground

Pin	Name	Type	On Module Termination	Description
B42	IDE_DATA11	IO-IDE		IDE/PATA interface
B43	IDE_DATA15	IO-IDE		
B44	IDE_DATA08	IO-IDE		
B45	IDE_DATA13	IO-IDE		
B46	IDE_DATA12	IO-IDE		
B47	IDE_DREQ	IO-LVTTL		
B48	IDE_DATA14	IO-IDE		
B49	IDE_DATA10	IO-IDE		
B50	IDE_DATA04	IO-IDE		
B51	GND	P		Ground
B52	IDE_A01	O-LVTTL		IDE/PATA interface
B53	USB_CLIENT	I-CMOS		USB2 client detection
B54	IDE_ACK#	O-LVTTL		IDE/PATA interface
B55	PCIE_WAKE#	I-LVTTL	PU 1kΩ V3.3	Standard I/O device wake event signal
B56	RESET#	O-3.3	PU 10kΩ V3.3S	System reset
B57	SMC_UART_RX	I-3.3		Maintenance port
B58	L_BKLTSEL	O		Selects backlight control (PWM vs. I^2C)
B59	PWR_BUTTON#	I-5	PU 10kΩ V5A	Power button
B60	GND	P		Ground
B61	USB7+	IO		USB7 (high speed only)
B62	USB7-			
B63	GND	P		Ground
B64	USB5+	IO		USB5
B65	USB5-			
B66	GND			Ground
B67	USB3+	IO		USB3
B68	USB3-			
B69	USB_OC0#	I-LVTTL	PU 10kΩ V3.3	USB0 over current
B70	GND			Ground
B71	USB1+	IO		USB1
B72	USB1-			
B73	GND			Ground
B74	LVDS_DATA3+	O-LVDS		LVDS data 3
B75	LVDS_DATA3-			

Pin	Name	Type	On Module Termination	Description
B76	GND			Ground
B77	LVDS_DATA0+	O-LVDS		LVDS data 0
B78	LVDS_DATA0-			
B79	USB_OC4#	I-LVTTL	PU 10kΩ V3.3	USB4 over current
B80	GND	P		Ground
B81	SDVO_RED+	O	C 0.1µF	SDVO data
B82	SDVO_RED-			
B83	GND	P		Ground
B84	SDVO_TVCLKIN+	I	C 0.1µF	SDVO external frequency reference
B85	SDVO_TVCLKIN-			
B86	GND	P		Ground
B87	SDVO_GREEN+	O	C 0.1µF	SDVO data
B88	SDVO_GREEN-			
B89	USB_OC1#	I-LVTTL	PU 10kΩ V3.3	USB1 over current
B90	GND	P		Ground
B91	SDVO_CLK+	O		SDVO clock reference
B92	SDVO_CLK-			
B93	GND	P		Ground
B94	PCIE1_PER-	I-PCIe		PCIe1 receive pair
B95	PCIE1_PER+			
B96	GND			Ground
B97	PCIE2_CLKREQ#	I-3.3	R 475Ω PU 10kΩ V3.3S	PCIe2 clock enable
B98	PCIE2_PET-	O-PCIe	C 0.1µF	PCIe2 transmit pair
B99	PCIE2_PET+			
B100	GND	P		Ground
B101	PCIE2_REFCLK+	O-HCSL		PCIe2 clock
B102	PCIE2_REFCLK-			
B103	GND	P		Ground
B104	PM_EN_S0#	O-3.3	PU 10kΩ V3.3A	Power state indicator
B105	PM_EN_PWR	O-3.3	PD 100kΩ	
B106	SMC_UART_TX	O-3.3		Maintenance port
B107	PM_EN_S3#	O-3.3	PU 10kΩ V3.3A	Power state indicator
B108	I2C_SDA	OD		I^2C bus
B109	I2C_SCL	OD		
B110	GND	P		Ground

J2: Docking Connector: Power

Board connector: 2x7 socket, 1 mm, Samtec CLM-107-02-LM-D

Carrier board connector: Samtec MW-07-03-G-D-095-085, 5 mm stacking height
Samtec MW-07-03-G-D-226-065, 8 mm stacking height

The Catalyst Module receives the power input and controls for interfacing with an external power supply on this docking connector. See Power Requirements, page 20 for a description of the Catalyst Module power supply.

Pin	Name	Pin	Type	On Module Termination	Description
1 3 5	V3.3		PI		3.3 V primary supply voltage
	Carrier_PWRGD	2	I-3.3	PU 10kΩ V3.3A	Indicator for input power voltages
	V_BATTERY	4	PI		RTC backup power
	V5A	6	PI		5 V “always” power
7 9	V5S		PI		5 V normal operating power
	V3.3A	8	PI		3.3 V “always” power
11 13	V3.3S		PI		3.3 V normal operating power
	GND	10 12 14	P		Ground

Disconnect the power input before removing the Catalyst Module. Removing the module from a powered carrier board may result in damage to both the carrier board and to the module.

J3: ITP Debug Port

Board connector: 24-pin FFC/FPC connector, 0.5 mm, Molex 52435-2472

Connector J3 provides an In-Target Probe (ITP) debug port for the Catalyst Module. Currently, this port is not supported for application use.

Pin	Name	Type	Description
1	XDP_BPM5#	O	
2	XDP_BPM4#	O	
3	GND	P	
4	XDP_BPM3#	O	
5	XDP_BPM2#	O	
6	GND	P	
7	XDP_BPM1#	O	
8	XDP_BPM0#	O	
9	GND	P	
10	XDP_H_PWRGD	O	
11	XDP_SLPIOVR#	O	
12	CLK_XDP	O	ITP debug port
13	CLK_XDP#	O	
14	V1.05S	PO	
15	XDP_H_CPURST#	O	
16	XDP_DBRESET	I	
17	GND	P	
18	XDP_TDO	O	
19	XDP_TRST#	I	
20	XDP_TDI	I	
21	XDP_TMS	I	
22	XDP_TCK1	I	
23	GND	P	
24	XDP_TCK	I	

System Specifications

Performance

The Catalyst Module and Catalyst Module XL are available in various versions based on processor speed, on-module DRAM, and operating temperature. The following table specifies the processor performance.

Parameter	Min	Typ.	Max	Units
Processor operating frequency (note 1)	1.1		1.6	GHz
Processor operating frequency (note 2)	1.1		1.33	GHz
Front side bus clock	400		533	MHz
Front side bus width		64		bit

Notes:

1. Performance specifications are for the Catalyst Module and Catalyst Module XL operating at commercial temperatures (0°C to 70°C).
2. Performance specifications are for the Catalyst Module XL operating at industrial temperatures (-40°C to +85°C).

Power

This section includes power specifications for the Catalyst Module.

Power Consumption

Using ACPI functionality, the Catalyst Module supports multiple modes of power saving operation. Although power consumption varies based on the level of processor activity and peripheral connections, values can be estimated for typical applications. The following table lists power consumption estimates.

Power Mode	Parameter	Min	Typ.	Max	Units
S0	Full operation		2	5	W
S3	Sleep			500	mW
S4	Hibernate			10	mW
S5	Power down			10	mW

Notes: Estimates given are expected values based upon typical applications.

Power Supply

The Catalyst Module requires 5 V and 3.3 V main input powers. On-module voltage regulators generate all voltages required by the processor and on-module circuitry. See Power Supply Architecture, page 21 for a description of the power supply.

Absolute Maximum Ratings

Input supply voltages 3.465 V, 5.25 V

Symbol	Parameter	Min	Typ.	Max	Units
System Power Inputs (note 3)					
V3.3	Primary supply voltage	3.135	3.3	3.465	V
$I_{V3.3}$			0.9	1.9	A
V3.3A	“Always” power	3.135	3.3	3.465	V
$I_{V3.3A}$			0.025	0.10	A
V3.3S	Normal operating power	3.135	3.3	3.465	V
$I_{V3.3S}$			0.13	1.0	A
V5A	“Always” power	4.75	5.0	5.25	V
I_{V5A}			0.0008	0.20	A
V5S	Normal operating power	4.75	5.0	5.25	V
I_{V5S}			0.1	0.4	A
V_BATTERY	RTC backup power (note 4)	2.4	3.3	3.5	V
$I_{V\_BATTERY}$			10	10	µA
Carrier_PWRGD					
V_{IH}	High-level input voltage	2.0	3.3		V
V_{IL}	Low-level input voltage			0.8	V
$T_{Carrier\_PWRGD}$	(note 5)			10	ms
PWR_BUTTON#					
V_{IH}	High-level input voltage	2.5	5		V
V_{IL}	Low-level input voltage			1.0	V
PM_EN_PWR					
V_{OH}	High-level output voltage	2.5	3.3		V
V_{OL}	Low-level output voltage			0.2	V

Notes:

3. The maximum currents per voltage rail include peak currents and are not indicative of aggregate power consumption during normal system operation.
4. V_BATTERY has 1 µF of bulk decoupling capacitance, load side of diode.
5. The carrier board must provide valid input power voltages and assert Carrier_PWRGD within $T_{Carrier\_PWRGD}$ after the assertion or de-assertion of any of the PM_EN_xxx signals.

Electrical

This section provides electrical specifications for the Catalyst Module. All specifications are based on typical values of the input power voltages given in Power, page 44. For details about termination of individual signals, see the signal connectors in Signal Headers, page 35.

Reset Circuitry

The Catalyst Module includes three reset signals. Two signals, RESET# and FP_RESET#, force a hard reset; while a third signal, H_INIT#, provides a soft reset. See Reset Signals, page 19 for a description of these signals.

Symbol	Parameter	Min	Typ.	Max	Units
RESET#					
V_{OH}	High-level output voltage	V_{CC}-0.4	3.3		V
I_{OH}	High-level output current	-4			mA
V_{OL}	Low-level output voltage			0.4	V
I_{OL}	Low-level output current	4			mA
FP_RESET# (note 6)					
V_{IH}	High-level input voltage	2.0	3.3		V
V_{IL}	Low-level input voltage			0.8	V
H_INIT# (note 7)					

Notes:

6. FP_RESET# is a 3.3 V open drain input. The module includes debounce circuitry and a 10kΩ pull-up resistor.
7. H_INIT# is a 1.05 V CMOS signal.

Intel High Definition Audio

The Intel SCH US15W supports the Intel HD Audio specification. Standard Catalyst Modules operate at 3.3 V signaling levels. A 1.5 V version is available as a volume production option. See Intel High Definition Audio, page 20 for a description of the audio interface.

The following specifications are from the Intel High Definition Audio Specification Revision 1.0 and are provided for reference only.

Symbol	Parameter	Min	Typ.	Max	Units
HDA					
V_{CC}	Supply voltage at 3.3 V signaling levels	3.135	3.3	3.465	V
V_{IH}	High-level input voltage	0.65 V_{CC}			V
V_{IL}	Low-level input voltage			0.35 V_{CC}	V
V_{OH}	High-level output voltage	0.9 V_{CC}			V
I_{OH}	High-level output current			-500	µA
V_{OL}	Low-level output voltage			0.10 V_{CC}	V
I_{OL}	Low-level output current			1500	µA
F_{HDA_SDIx}	Data rate		24		Mbps

Embedded Controller

The embedded controller provides an external I^2C bus, a maintenance port, and multiple discrete I/O signals including GPIO, LPCPD#, THERM_ALERT, and PM_EN_Sx#. See Embedded Controller, page 12 for a description of these I/O capabilities.

Symbol	Parameter	Min	Typ.	Max	Units
LPCPD#, THERM_ALERT					
V_{IH}	High-level input voltage	1.7	3.3		V
V_{IL}	Low-level input voltage			0.8	V
V_{OH}	High-level output voltage	2.4			V
I_{OH}	High-level output current			-4	mA
V_{OL}	Low-level output voltage			0.45	V
I_{OL}	Low-level output current			4	mA
T_{THERM_ALERT}	External BIOS enable (note 8)	200			ns
GPIO					
V_{IH}	High-level input voltage	1.7	3.3		V
V_{IL}	Low-level input voltage			0.8	V
V_{OH}	High-level output voltage	V_{CC}-0.2			V
I_{OH}	High-level output current			-0.1	mA
V_{OL}	Low-level output voltage			0.2	V
I_{OL}	Low-level output current			0.1	mA
PM_EN_Sx#					
V_{OH}	High-level output voltage	V_{CC}-0.4	3.3		V
I_{OH}	High-level output current	-4			mA
V_{OL}	Low-level output voltage			0.4	V
I_{OL}	Low-level output current	4			mA

Notes:

8. A low level driven by the carrier board on THERM_ALERT immediately preceding de-assertion of RESET# enables the external BIOS option.

Clock Generator

The Catalyst Module provides two PCIe x1 interfaces with an on-module clock generator supplying the PCIe clock for each interface. Two additional input signals, PCIEx_CLKREQ#, individually control each reference clock. See PCI Express Bus, page 14 for a description of the PCIe interfaces.

Symbol	Parameter	Min	Typ.	Max	Units
PCIEx_REFCLK (note 9)					
F_{PCIEx_REFCLK}	Frequency		100		MHz
V_{OH}	High-level output voltage	600	700	850	mV
V_{OL}	Low-level output voltage	-150	0	27	mV
PCIEx_CLKREQ#					
V_{IH}	High-level input voltage	2.0	3.3	3.6	V
V_{IL}	Low-level input voltage	-0.3		0.8	V

Notes:

9. PCIE1_REFCLK +/- and PCIE2_REFCLK+/- are HCSL outputs.

General

This section provides general specifications for the Catalyst Module.

Crystal Frequencies

Agencies certifying the Catalyst Module for compliance for radio-frequency emissions typically need to know the frequencies of on-system oscillators. The following table lists the frequencies of all crystals on the Catalyst Module and carrier board.

Crystals	Device	Typ.	Units
Module			
X1	RTC	32.768	kHz
X2	Clock Generator	14.31818	MHz
X4	Embedded Controller	14.7456	MHz

Real-Time Clock

The Intel SCH US15W includes a RTC function that retains the system date and time. See Non-Volatile Memory, page 12 for a description of the RTC function.

Parameter	Typ.	Units
Accuracy per month @ 25°C	+/-55	sec

Environmental

The Catalyst Module is available in commercial and extended operating temperatures with no external cooling required.

Parameter	Min	Typ.	Max	Units
Commercial operating temperature	0		+70	°C
Industrial, extended operating temperature	-40		+85	°C
Storage temperature	-40		+85	°C
Relative humidity, non-condensing	5		95	%

Appendix A – Reference Information

Product Information

Product notices, updated drivers, support material:

www.eurotech.com

Intel

Information about the Intel Atom processor, Intel System Controller Hub US15W, Intel High Definition Audio specification:

www.intel.com

Trusted Computing Group

Trusted Computer Group specifications:

www.trustedcomputinggroup.org

PCI SIG

PCI Express specification:

www.pcisig.com

USB

Universal Serial Bus specification and product information:

www.usb.org

SDIO Card

SD Card Association and SDIO specification:

www.sdcard.org

MMC Card

JEDEC MMC 4.0 specification:

www.jedec.org

ACPI Specification

Information about the ACPI specification:

www.acpi.info

Appendix B – RoHS Compliance

EUROTECH

The Restriction of the use of certain Hazardous Substances (RoHS) Directive came into force on 1st July 2006. This product shall be designed using RoHS compliant components, and manufactured to comply with the RoHS Directive.

Eurotech has based its material content knowledge on a combination of information provided by third parties and auditing our suppliers and sub-contractor's operational activities and arrangements. This information is archived within the associated Technical Construction File. Eurotech has taken reasonable steps to provide representative and accurate information, though may not have conducted destructive testing or chemical analysis on incoming components and materials.

Additionally, packaging used by Eurotech for its products complies with the EU Directive 2004/12/EC in that the total concentration of the heavy metals cadmium, hexavalent chromium, lead and mercury do not exceed 100ppm.

Appendix C – Board Revision

This guide applies to the current revision of the module as given in the following section.

Identifying the Board Revision

The revision number is printed on the underside of the printed wiring board. That number is 170122-200Rx for the Catalyst Module and 170123-300Rx for the Catalyst Module XL. The “x” indicates the revision level of the PWB.

Catalyst Module Revision History

The following is an overview of the revisions to the Catalyst Module.

Revision 1

Initial release

Revision A

Improved manufacturability

Connects bottom side EMI ring

Changes connection of SPI Flash internal to the Embedded Controller circuitry

Revision B

Removes TPM from the LPC bus and adds it as an optional feature on the SMBus

Implements changes to support updated silicon for the Intel Atom processor and Intel SCH US15W chipset

Revision C

Replaces 1.05 V, 1.5 V, and 1.8 V power supplies with discrete solutions

Changes circuitry to reduce surge current on V3.3A as the module switches from power state S5 to S3

Revision D

Changes decoupling capacitance on 1.05 V, 1.5 V, and 1.8 V to improve design margin

Changes start-up of 1.5 V and 1.8 V power supplies to reduce surge current on VBATA

Catalyst Module XL Revision History

The following is an overview of the revisions to the Catalyst Module XL.

Revision 1

Initial release

Revision A

Implements routing changes to improve design margin

Adds jumper J10 for programming the embedded controller

Revision B

Removes TPM from the SMBus and adds it as an optional feature on the LPC bus

Appendix D – Development Kit

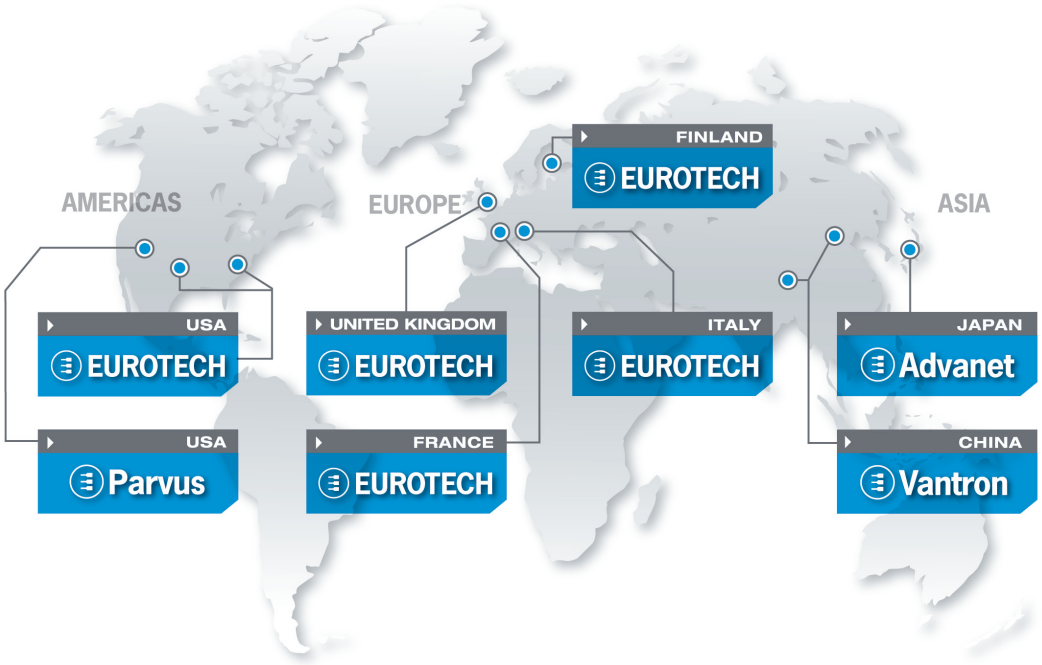
Catalyst Module Development Kits are designed to get the developer up and running quickly. This configuration allows you to become familiar with the Catalyst Module functionality prior to customization for your specific application.

The development kit includes the Catalyst Module, the carrier board, and supporting peripheral devices. To provide flexibility and allow development across a broad spectrum of end-use applications, the carrier board maximizes the Catalyst Module functionality and implements many industry-standard interfaces.

For a complete description of the Catalyst Module Development Kit, refer to the Catalyst Module Development Kit User Manual (Eurotech document 110122-3001).

(This page intentionally blank)

Eurotech Worldwide Presence



EUROTECH

AMERICAS

USA

EUROTECH
Toll free +1 888.941.2224
Tel. +1 301.490.4007
Fax +1 301.490.4582
E-mail: sales.us@eurotech.com
E-mail: support.us@eurotech.com
Web: www.eurotech-inc.com

PARVUS
Tel. +1 800.483.3152
Fax +1 801.483.1523
E-mail: sales@parvus.com
E-mail: tsupport@parvus.com
Web: www.parvus.com

EUROPE

Italy

EUROTECH
Tel. +39 0433.485.411
Fax +39 0433.485.499
E-mail: sales.it@eurotech.com
E-mail: support.it@eurotech.com
Web: www.eurotech.com

United Kingdom

EUROTECH
Tel. +44 (0) 1223.403410
Fax +44 (0) 1223.410457
E-mail: sales.uk@eurotech.com
E-mail: support.uk@eurotech.com
Web: www.eurotech.com

France

EUROTECH
Tel. +33 04.72.89.00.90
Fax +33 04.78.70.08.24
E-mail: sales.fr@eurotech.com
E-mail: support.fr@eurotech.com
Web: www.eurotech.com

Finland

EUROTECH
Tel. +358 9.477.888.0
Fax +358 9.477.888.99
E-mail: sales.fi@eurotech.com
E-mail: support.fi@eurotech.com
Web: www.eurotech.com

ASIA

Japan

ADVANET
Tel. +81 86.245.2861
Fax +81 86.245.2860
E-mail: sales@advanet.co.jp
E-mail: tsupport@advanet.co.jp
Web: www.advanet.co.jp

China

VANTRON
Tel. + 86 28.85.12.39.30
Fax +86 28.85.12.39.35
E-mail: sales@vantrontech.com.cn
E-mail: support.cn@eurotech.com
Web: www.vantrontech.com.cn

EUROTECH

www.eurotech.com